

Model: Mission Hills/Sawgrass

PCB Ver: A00

PCB Number: 10097-1

SCH Ver: 06

PCBA:

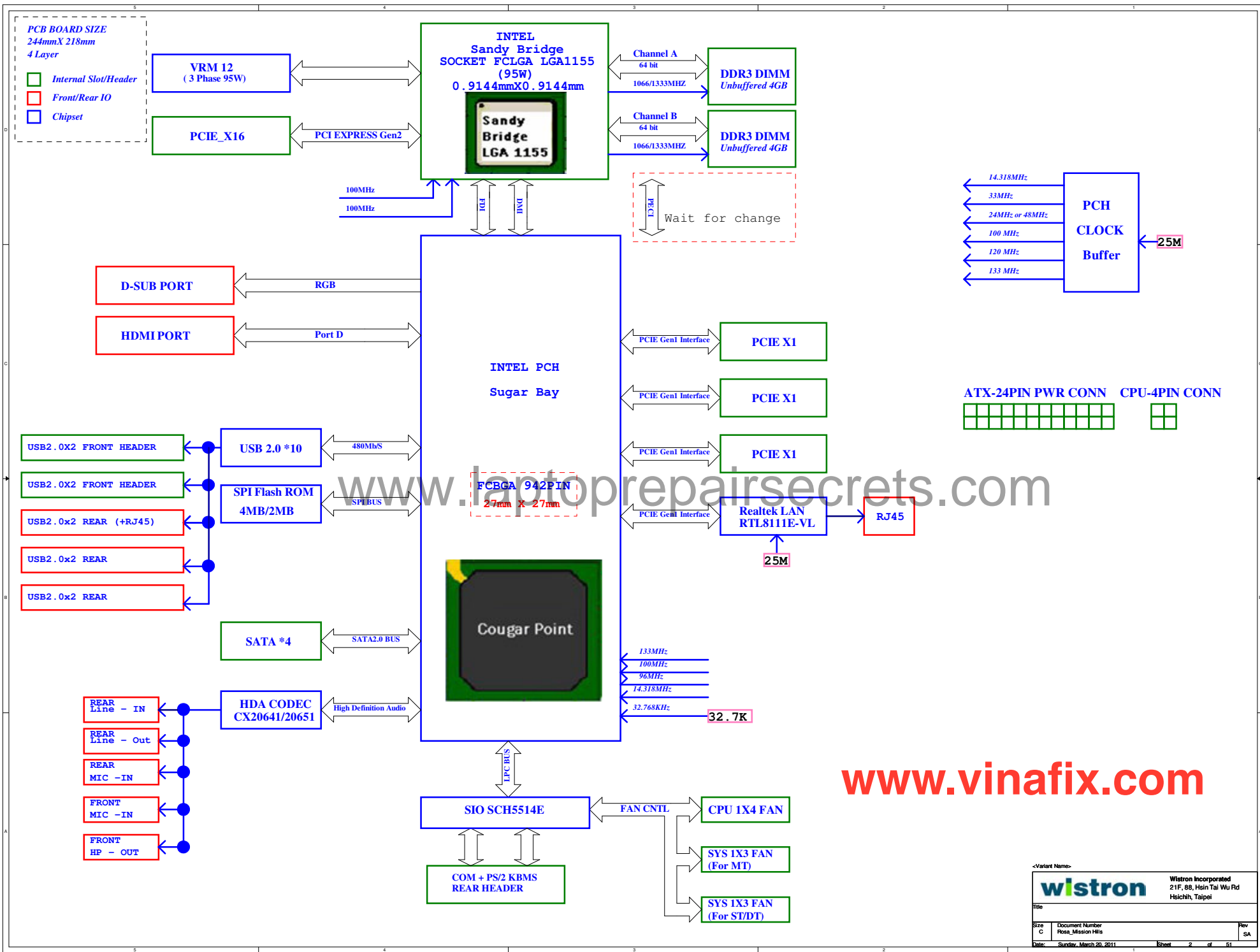
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09	CLOCK GEN - CK505	
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48	SYSTEM POWER	
49	CPU VTT & CPU SA	
50	CPU VRD 12-1 & CPU AXG	
51	CPU_VRD 12-2	

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PCB BOARD SIZE
4 Layers
244mmX 218mm

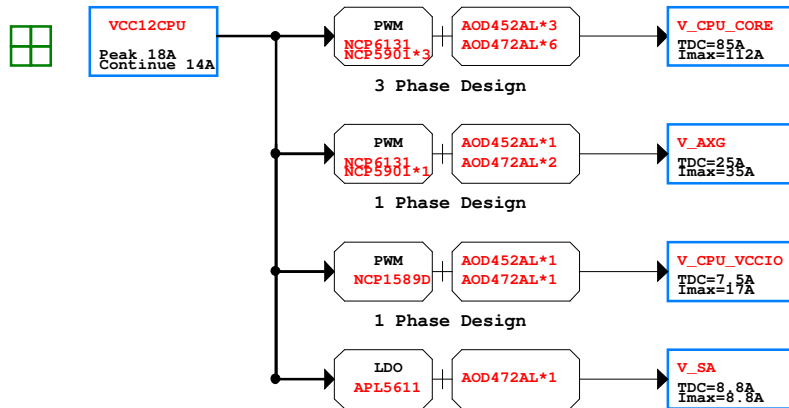
BOM Configuration
Unmount: (R)
Unmount after MP (X)

SB BUILD
Sugar Bay :
LGA1155 : Sandy Brighe
Chipset : Cougar Point H61
LAN : Gb LAN RTL8151ED

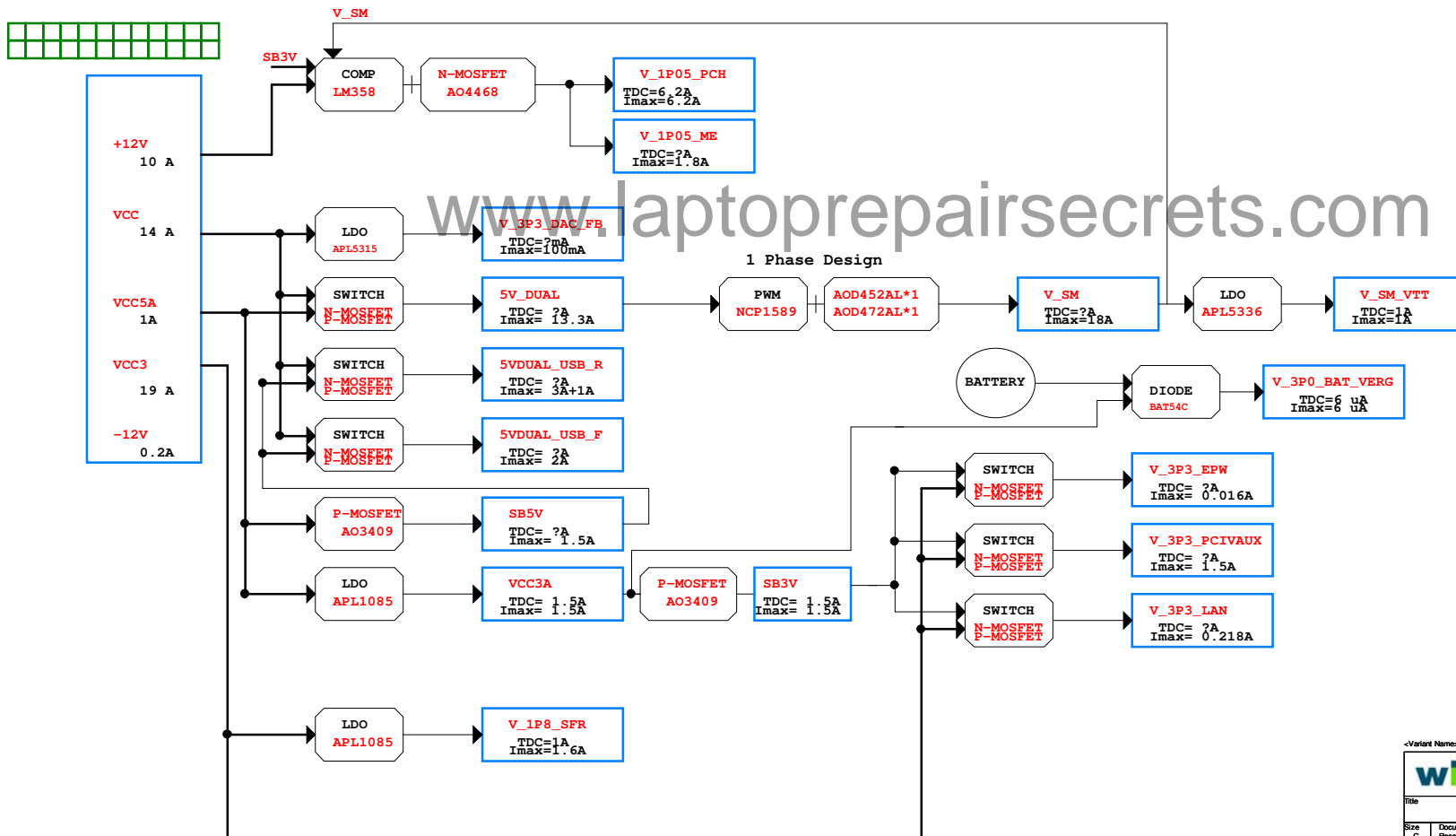


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CPU 2X2 POWER CONN



ATX 2X12 POWER CONN



<Variant Name>

wistron

Wistron Incorporated
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Hsichih, Taipei

Title

Size

C

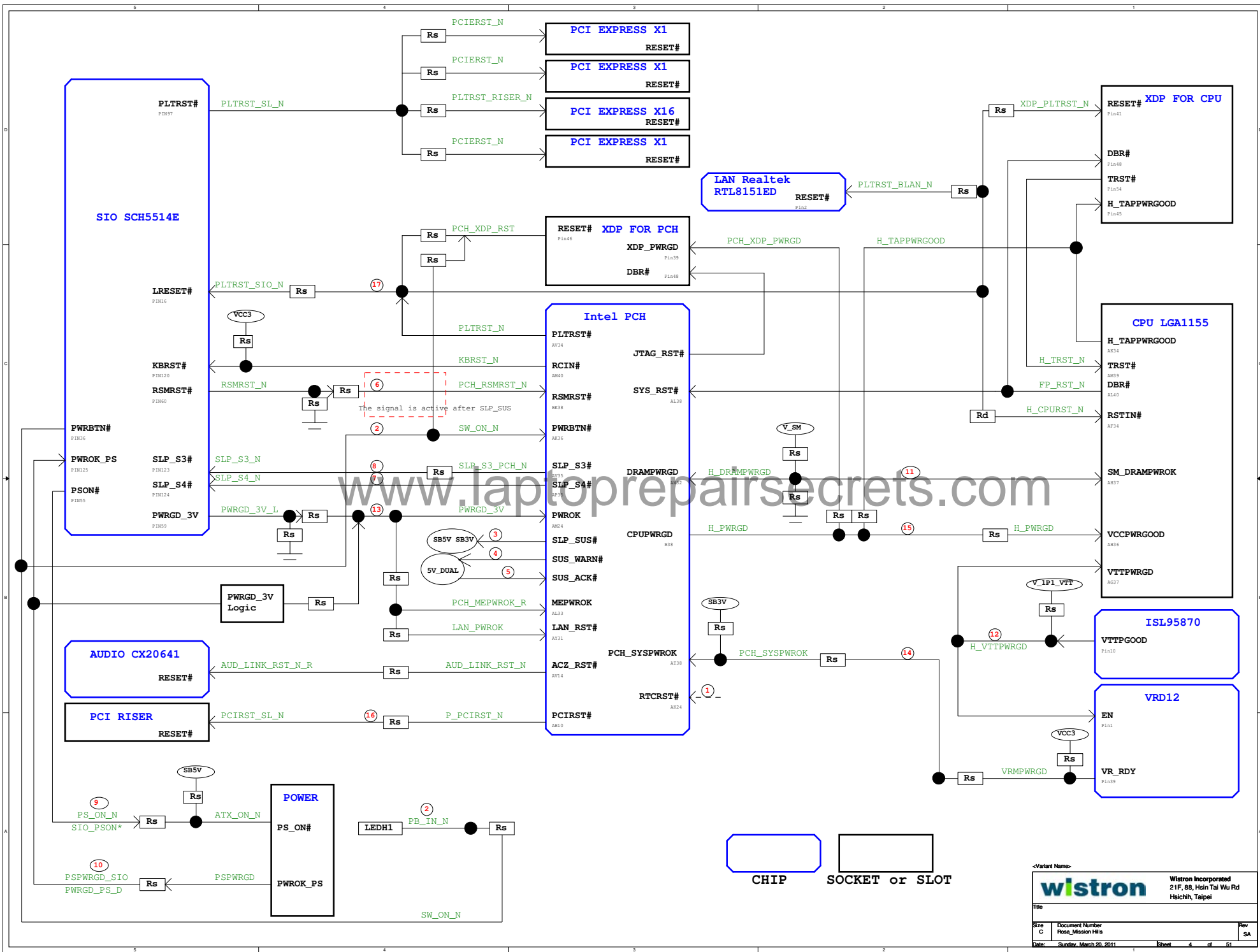
Document Number
Pesa_Mission Hills

Date: Sunday, March 20, 2011

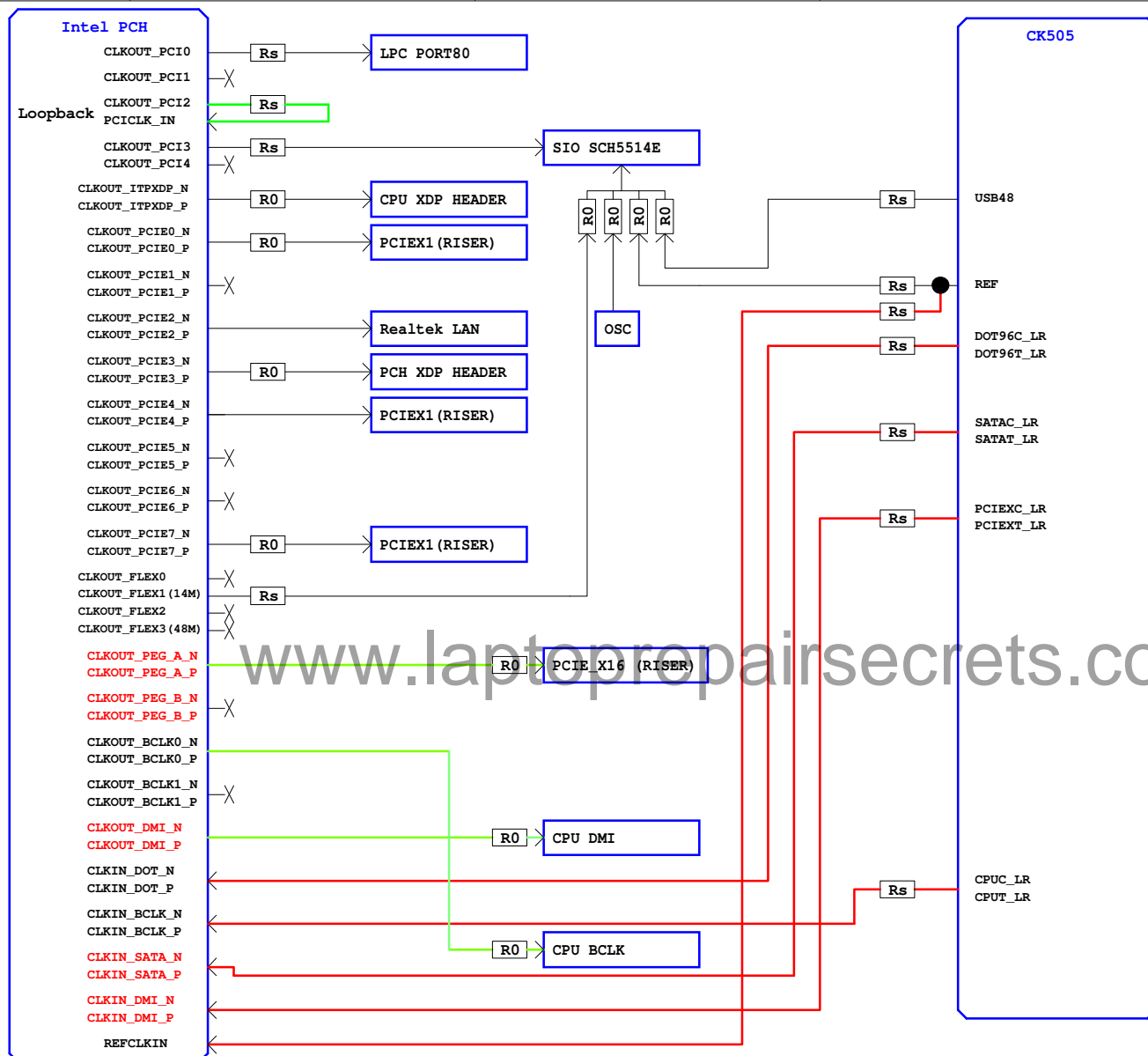
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Rev

SA

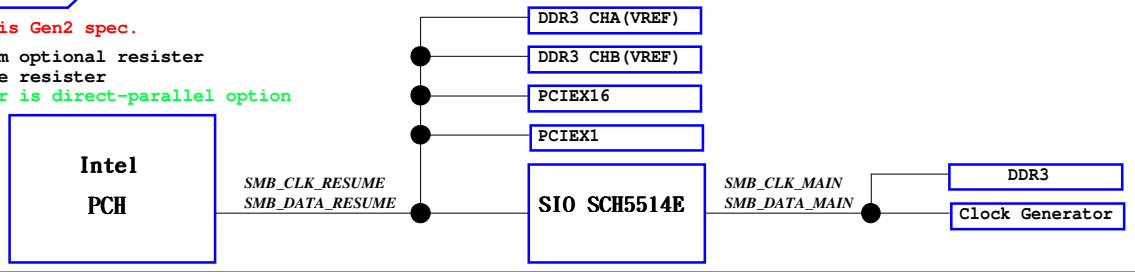


CHIP SOCKET or SLOT

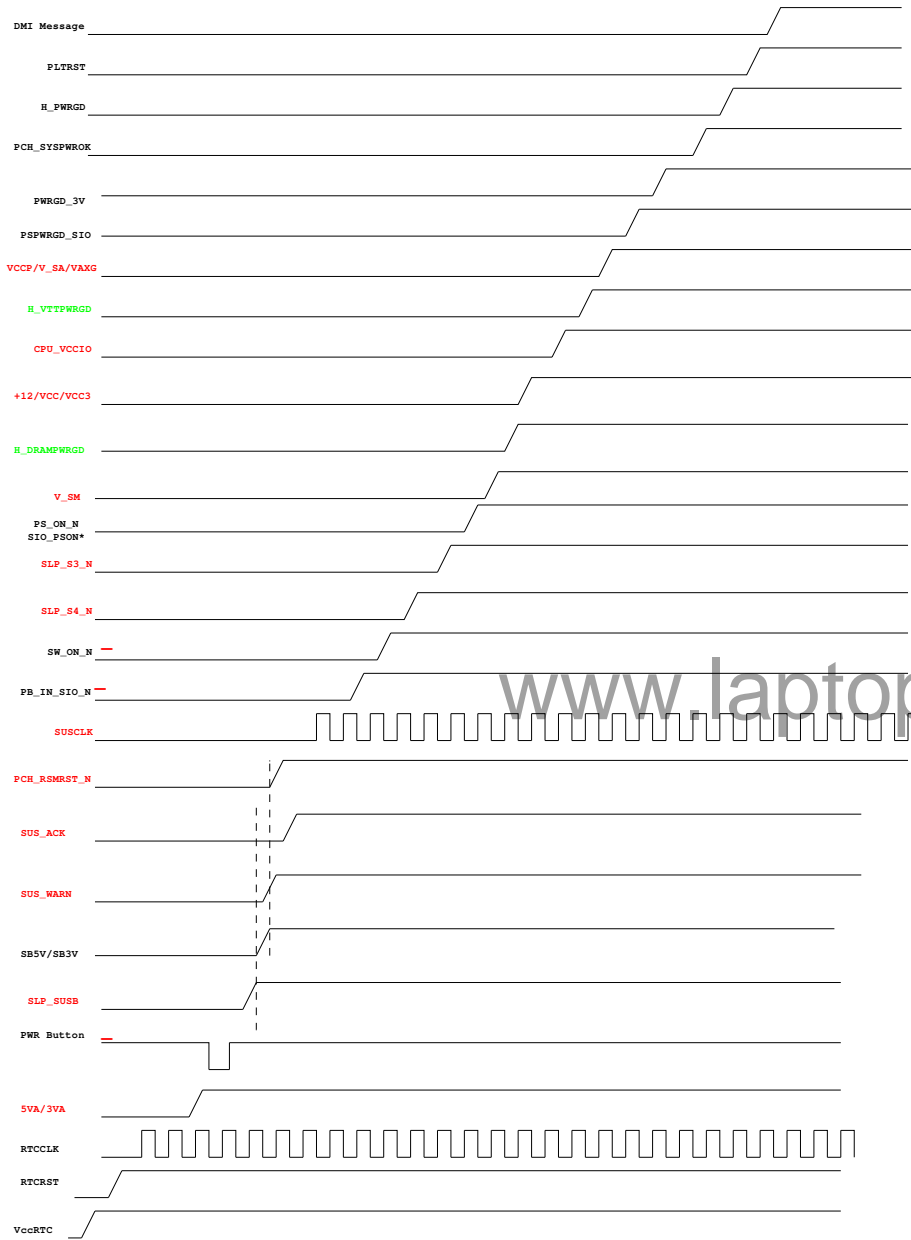


BTM: Buffer Through Mode
 Need CK505 to provide 4 clock to PCH
 FCIM: Full Clock Intergration Mode
 Remove CK505

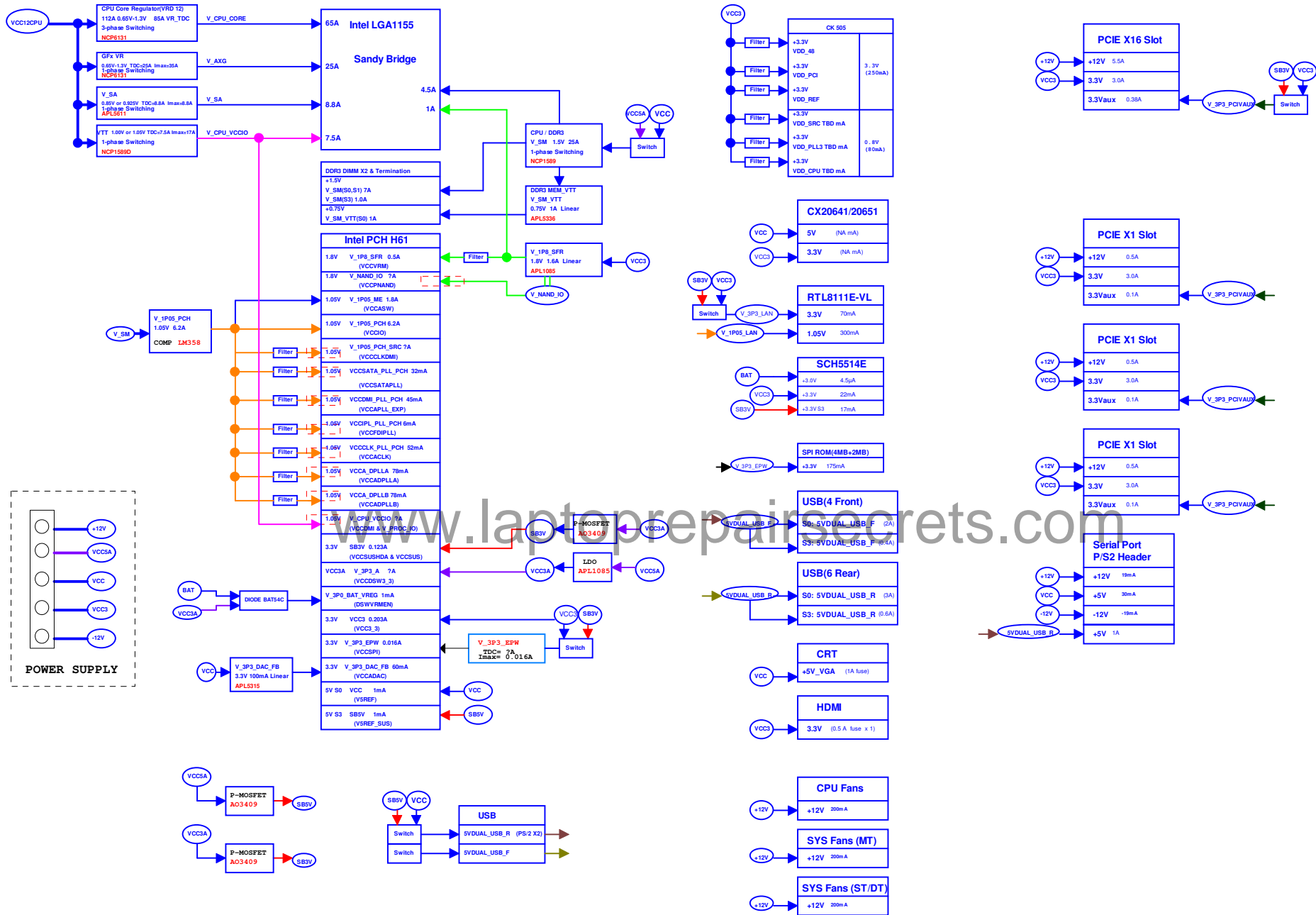
Note: Red Color is Gen2 spec.
 Note: R0 is 0 ohm optional resistor
 Note: Rs is serie resistor
 Note: Green Color is direct-parallel option



POWER ON SEQUENCE



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PCH (H61)

PIN NAME	Pin#	POWER WELL	USAGE	BIOS Post Value	Default Type	Notes
GPIO0	AW52	MAIN	PCD REQ_N	GPI (No Use)	GPI	10K P/U to VCC3 MAIN
GPIO1	BR19	MAIN	HDMI_DETECT	GPI (Low: NO HDMI, High: HDMI detect)	GPI	1 P/U 20K
GPIO2	BN8	MAIN	P_INT_E_N	GPI (No Use)	GPI	Unused,8.2K P/U to VCC3 MAIN
GPIO3	AV9	MAIN	P_INTF_N	GPI (No Use)	GPI	Unused,8.2K P/U to VCC3 MAIN
GPIO4	BT15	MAIN	P_INTG_N	GPI (No Use)	GPI	Unused,8.2K P/U to VCC3 MAIN
GPIO5	BR4	MAIN	P_INTH_N	GPI (No Use)	GPI	Unused,8.2K P/U to VCC3 MAIN
GPIO6	BA22	MAIN	TACH2	GPI (No Use)	GPI	Unused,10K P/U to VCC3 MAIN,1 P/U 20K
GPIO7	BR16	MAIN	TACH3	GPI (No Use)	GPI	Unused,10K P/U to VCC3 MAIN,1 P/U 20K
GPIO8	BP51	RESUME	IO_SMI_N	GPI (IO_SMI_N)	GPO	10K P/U to SB3V
GPIO9	BJ41	RESUME	USB_OC5_R_N	NATIVE	Native	USB OVER CURRENT
GPIO10	BT45	RESUME	USB_OC6_R_N	NATIVE	Native	10K P/U to SB3V
GPIO11	BM49	RESUME	LPC_PME_N	GPI (LPC_PME_N)	Native	LPC_PME_N,10K P/U to SB3V
GPIO12	BK50	RESUME	PCH_HEATSINK_DETECT (Reserved)	GPI (Low: PCH Heatsink detected, High: No PCH Heatsink)	Native	10K P/U to SB3V
GPIO13	BA25	RESUME	PWR_CLEAR	GPI (High: Normal, Low: Clear Password)	GPI	10K P/U to SB3V, with a Jumper to GND
GPIO14	BM45	RESUME	USB_OC7_R_N	NATIVE	Native	10K P/U to SB3V
GPIO15	BM55	RESUME	USB_OC7_R_N	GPO (Unused)	GPO	1 P/D 20K (Strapping)
GPIO16	AU56	MAIN	FB_USB2_DET	GPI (Low: Front USB detected, High: No Front USB)	GPI	10K P/U to VCC3 MAIN
GPIO17	BT17	MAIN	TACH0	GPI (No Use)	GPI	Unused,10K P/U to VCC3 MAIN
GPIO19	AV52	MAIN	SATA1GP	GPI (No Use)	GPI	Unused,10K P/U to VCC3 MAIN (Strapping)
GPIO20	AV43	MAIN	BOARD_ID_0	GPI (No Use)	Native	10K P/U to VCC3 MAIN,10K P/U to GND
GPIO21	BC54	MAIN	FB_USB1_DET	GPI (Low: Card Reader detected, High: No Card Reader)	GPI	FB_USB1_DET,10K P/U to VCC3 MAIN
GPIO22	BA53	MAIN	BIOS_RCY_GP22	GPI (No Use)	GPI	BIOS_RCY_GP22,10K P/U to VCC3 MAIN
GPIO23	BA20	MAIN	LPC_DRQ1_N	GPI (Not required for test)	Native	Unused,1 P/U 20K
GPIO24	BP53	RESUME	H_SKT0CC_R_N	GPI (Low: CPU detected, Floating: No CPU)	GPO	H_SKT0CC_R_N,1K(R) P/U to +3P3V, AUX,10K(R) P/D to GND
GPIO27	BJ43	ep Sleep Power W	PCH_GP27_PU	GPI (Unused)	GPI	10K P/U to V_3P3_A
GPIO28	BJ55	RESUME	PCH_GP28_PU	GPO (Unused)	GPO	10K(R) P/U to V_3P3_A
GPIO29	BM49	RESUME	SLP_LAN_N	GPO (S0/S5 Low, S3 High)	Native	LAN Enable/Disable
GPIO30	BU46	RESUME	SUS_WARNB	S5 Low to turn off LAN power in S5	GPI	Function Pin
GPIO31	BG43	ep Sleep Power W	PCH_GP31_PU	GPI (Unused)	GPI	10K P/U to V_3P3_A
GPIO32	BC56	MAIN	EXT_MUTEW	GPO (50 High, S3/S5 Low)	GPO	External Mute
GPIO33	BC25	MAIN	SOP_ENABLE_GP33	S3/S5 Low to mute all ports	GPO	10K P/U to VCC3 MAIN,1 P/U 20K
GPIO34	BL56	MAIN	SPK_DETECT	Unused (GPO)	GPI	SPK_DETECT,10K P/U to VCC3 MAIN
GPIO35	BJ57	MAIN	SPK_MUTEW	GPI (50 High, S3/S5 Low)	GPO	SPK_MUTEW,10K P/U to VCC3 MAIN
GPIO36	BB55	MAIN	SATA2GP	S3/S5 Low to mute external speaker	GPI	SPK_MUTEW,10K P/U to VCC3 MAIN
GPIO37	BA53	MAIN	SATA3GP	GPI (Unused)	GPI	Unused,10K(R) P/U to VCC3 MAIN
GPIO38	BE54	MAIN	CHASSIS_ID_0	GPI (Unused)	GPI	Unused,10K P/U to VCC3 MAIN
GPIO39	BF55	MAIN	CHASSIS_ID_1	GPI (Pis refer to CHASSIS_ID table)	GPI	CHASSIS_ID_0,10K P/U to VCC3 MAIN
GPIO40	BD41	RESUME	USB_OC1_R_N	GPI (Pis refer to CHASSIS_ID table)	GPI	CHASSIS_ID_1,10K P/U to VCC3 MAIN
GPIO41	BG41	RESUME	USB_OC2_R_N	Native (OC1W)	Native	USB OVER CURRENT
GPIO42	BK43	RESUME	USB_OC3_R_N	Native (OC2W)	Native	USB OVER CURRENT
GPIO43	BF43	RESUME	USB_OC4_R_N	Native (OC3W)	Native	10K P/U to SB3V
GPIO44	BL54	RESUME	LAN_EN	Native (OC4W)	Native	USB OVER CURRENT
GPIO45	AV44	RESUME	1_WATT_CTRL_1	GPI (High: LAN enable, Low: LAN disable)	Native	10K P/U to SB3V,10K(R) P/D to GND
GPIO46	BP55	RESUME	INTRU_DET	GPI (High: Slim Tower, Low: Mini Tower)	Native	INTRU_DET,10K P/U to SB3V,1K(R) P/D to GND
GPIO48	AW53	MAIN	MTST_ID	GPI (High: Slim Tower, Low: Mini Tower)	GPI	MTST_ID,10K P/U to VCC3 MAIN
GPIO49	BA56	MAIN	VGA_DET	GPI (High: VGA detected, Low: No VGA)	GPI	VGA_DET,10K P/U to VCC3 MAIN
GPIO50	BT5	MAIN	P_REQ_N1	Native (Unused)	Native	Function Pin,8.2K P/U to VCC3 MAIN
GPIO51	AV8	MAIN	P_REQ_N1	Native (Unused)	Native	Strap Pin,1K(R) P/D GND,1 P/U 20K
GPIO52	BR8	MAIN	P_REQ_N2	Native (Unused)	Native	Function Pin,8.2K P/U to VCC3 MAIN
GPIO53	BU12	MAIN	P_REQ_N2	Native (Unused)	Native	Strap Pin,1K(R) P/D GND,1 P/U 20K
GPIO54	AV11	MAIN	P_REQ_N3	Native (Unused)	Native	Function Pin,8.2K P/U to VCC3 MAIN
GPIO55	BE2	MAIN	P_GNT_N3	Native (Unused)	Native	Strap Pin,1K(R) P/D GND,1 P/U 20K
GPIO57	BT53	RESUME	ME_CNTL	GPI (High: Suspend OK, Low: Suspend NG)	GPI	Unused,10K(R) P/U to SB3V,47K P/D GND
GPIO58	BJ46	RESUME	SMLCLK_PCH	Native (Unused)	Native	SMLCLK_PCH,10K P/U to SB3V
GPIO59	BM43	RESUME	USB_OC0_R_N	Native	Native	USB OVER CURRENT
GPIO60	BU49	RESUME	SMLALERT_PCH	Native (Unused)	Native	SMLALERT_PCH,2.2K P/U to SB3V
GPIO61	BM54	RESUME	SUS_STAT_N	Native	Native	W_DISABLE_N,10K P/U (R) to SB3V
GPIO62	BA47	RESUME	SUSCLK	Native	Native	Unused, TP
GPIO63	BD50	RESUME	SLP_S5_N	Native	Native	Unused, TP
GPIO64	AT9	MAIN	Test point (CLKOUTFLEX0)	GPI (Unused)	Native	Unused,1 P/D 20K
GPIO65	BA5	MAIN	CK_14M_FLEX	Native (14.318MHz CLK)	Native	14.318MHz CLK for SIO1 P/D 20K
GPIO66	AW5	MAIN	Test point (CLKOUTFLEX2)	GPI (Unused)	Native	Unused,1 P/D 20K
GPIO67	BA2	MAIN	BOARD_ID_1	GPI (Reserved, Board ID Table)	Native	P/D 20K
GPIO68	BU16	MAIN	FP_DETECT (Palm Beach MT/DT Only)	GPI (Low: PWR cable detected, High: No PWR cable)	TBD	10K P/U to VCC3 MAIN
GPIO69	BM18	MAIN	TACH5	Unused	TBD	Unused,10K P/U to VCC3 MAIN
GPIO70	BN17	MAIN	SERIAL_DETECT	GPI (Low: COM Port/KBMS detected, High: No COM/KBMS)	GPI	SERIAL_DETECT,10K P/U to VCC3 MAIN
GPIO71	BP15	MAIN	FP_AUD_DETECT	GPI (Low: Front Audio detected, High: No Front Audio)	GPI	FP_AUD_DETECT,10K P/U to VCC3 MAIN
GPIO72	AV46	RESUME	USB_PWR_CRL1	GPO (S0/S3 High, S5 Low) If board ID is 11 S3 High to turn on USB 5V, S5 Low to turn off USB 5V	GPO	USB_PWR_CRL1,10K P/U to SB3V
GPIO74	BR46	RESUME	SML1ALERT_PCH	GPO (S0/S3 Low, S5 High) If board ID is 00 S0 Low to turn on USB 5V, S5 High to turn off USB 5V	GPO	USB_PWR_CRL1,10K P/U to SB3V
GPIO75	BR46	RESUME	SMLIDATA_PCH	Native (Unused)	Native	SML1ALERT_PCH,10K P/U to SB3V
				Native (Unused)	Native	SMLIDATA_PCH,10K P/U to SB3V

SCH5514E

GPIO#	Mux Function	GPIO Function	BIOS Post Value	BIOS Default value	BIOS output type	Pull up/down
GP8051_1	DDC_DATA_2P5V	DIAG_LED1	GPIO	Unused, follow original function	GPIO	Open Drain
GP8051_2	DDC_CLK_5V	DIAG_LED3	GPIO	Unused, follow original function	GPIO	Open Drain
GP8051_3	DDC_DATA_5V	DIAG_LED3	GPIO	Unused, follow original function	GPIO	Open Drain
GP8051_4	DDC_CLK_2P5V	DIAG_LED4	GPIO	Unused, follow original function	GPIO	Open Drain
GP8051_5	PWRBT1W	Unused	Native	follow original function	Native	Push Pull
GP8051_6	R1W	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP8051_7	CTS2W	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP8051_8	DSR2W	SMLIDATA_PCH_SIO	GPO (H)	Unused, set as "GPO" to prevent floating	GPIO	Push Pull
GP8051_9	DCD2W	SMLCLK_PCH_SIO	GPO (H)	Unused, set as "GPO" to prevent floating	GPIO	Push Pull
3P8051_10	DCD1W	Unused	Native	follow original function	Native	Input
3P8051_11	DSR1W	Unused	Native	follow original function	Native	Input
3P8051_12	RX01	Unused	Native	follow original function	Native	Input
3P8051_14	RX01	Unused	Native	follow original function	Native	Push Pull
3P8051_16	CTS1W	Unused	Native	follow original function	Native	Input
3P8051_16	DSR1W	Unused	Native	follow original function	Native	Push Pull
3P8051_17	R1W	Unused	Native	follow original function	Native	Input
GP10	SLP_S3W	Unused	Native	follow original function	Native	Push Pull
GP11	SLP_S5W	Unused	Native	follow original function	Native	Push Pull
GP14	HD_LEDW	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP21	P16IO31W	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP22	P12/MRT1W/SCSW	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP23	LATCHED_BF_CUT	Unused	Native	follow original function	Native	Push Pull
GP25	SCLK	Unused	Native	follow original function	Native	Open Drain
GP26	SCLK_1	Unused	Native	follow original function	Native	Open Drain
GP31	SECONDARY_HDW	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP33	PRIMARY_HDW	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP35	SDATLE01	Unused	Native	follow original function	Native	Open Drain
GP36	KBORSTW	Unused	Native	follow original function	Native	Open Drain
GP37	A20GATE	Unused	Native	follow original function	Native	Open Drain
GP40	DRIVEN0	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP41	IO_PMEW	Unused	Native	follow original function	GPIO	Open Drain
GP42	SDAT_1YD_SMIW	Unused	Native	follow original function	Native	Open Drain
GP52	RYD2	SLOT0CC_N	Native	reserve, follow original function	GPIO	Push Pull
GP53	TXD2	COPEN_N	Native	reserve, follow original function	GPIO	Push Pull
GP55	RTCWDR0RC	CPURST_IN	Native	reserve, follow original function	GPIO	Push Pull
GP57	DTB2W	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP60	YELLOW	Unused	Native	follow Power LED behavior function S0/S1: High S3: Low S4/S5: High boot failure (No Post): Low boot failure (Post) Blinking	Native	Open Drain
GP61	GREEN	Unused	Native	follow Power LED behavior function S0/S1: Low S3: High S4/S5: High boot failure (No Post): High boot failure (Post): High	Native	Open Drain
GP75	DE_RSTDRWV	IO_SMI_N	GPO (IO_SMI)	set as "GPO" for SMI function	Native	Open Drain
GP76	PCI_RST_3YSW	Unused	Native	follow original function	Native	Push Pull
GP77	PCI_RST_SL0TSW	Unused	Native	follow original function	Native	Push Pull
GP80	PS_ONW	Unused	Native	follow original function	Native	Open Drain
GP81	BACKFEED_CUTW	Unused	Native	follow original function	Native	Open Drain
GP82	None	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP83	PWR_S0D0_3V	Unused	Native	follow original function	Native	Push Pull
GP84	RSRSTW	Unused	Native	follow original function	Native	Push Pull

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New

SA

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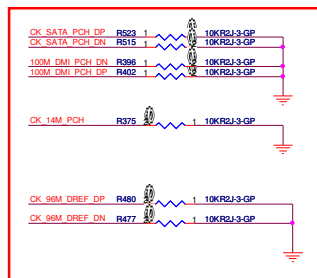
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PCH Buffer CLOCK

22 CK_96M_DREF_DP
22 CK_96M_DREF_DN
21 CK_SATA_PCH_DP
21 CK_SATA_PCH_DN
22 100M_DM_PCH_DP
22 100M_DM_PCH_DN

14M CLOCK

20 CK_14M_PCH



Terminate PCH CLK Inputs

Remove CLK GEN
Use PCH Internal CLK
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CLOCK

20 CK_PE_100M_MCP_DP
20 CK_PE_100M_MCP_DN

CPU_SA

49 VCCA_VID
49 VCCA_SENSE

CPU_VTT

49 VCCO_SEL
49 VCCO_SENSE
49 VSSO_SENSE

CPU_AXG

50 VCCA_SENSE
50 VSSA_SENSE

CPU_VCORE

50 VCC_SENSE
50 VSS_SENSE

ITP

14 H_TDO
14 H_TDI
14 H_TCK
14 H_TMS
14 H_TRST_N
14 H_PROG_N
14 H_PREG_N

14 XDP_DBRESET_N
14 CK_XDP_S_DN
14 CK_XDP_S_DP

14 H_BPM0
14 H_BPM1
14 H_BPM2
14 H_BPM3
14 H_BPM4
14 H_BPM5
14 H_BPM6
14 H_BPM7

14.36 H_CPURST_N

OTHER

14.19.36 PLTRST_N
14.19 H_PWRGD
19 FP_RST_DBR_N

19.46 H_DRAMPWRGD
21.36 H_PECI
36.50 H_PROCHOT_N

21 H_THERMTRIP_N
21 H_PM_SYNC_0
19.36 H_SKT0CC_N
14.36 H_CPURST_N

23 H_SNB_N

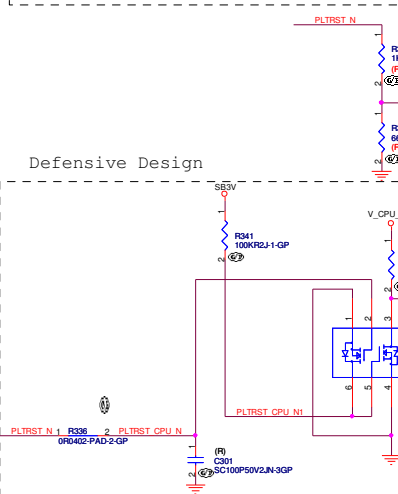
19.26.32.36.41 SMB_CLK_RESUME
19.26.32.36.41 SMB_DATA_RESUME

14 TPEV_SNB_POUDEBUG_0

03/21: follow C811-0 from the CPU0 to XDP 1

MINIMIZE STUB BETWEEN THESE AND RESISTORS AT SIM PAGE
PLACE IN CN3 AREA

H_VDSOCK_VR R355 1 0R04 PAD-2-GP H_VDSOCK
H_VDSOUT_VR R350 1 0R04 PAD-2-GP H_VDSOUT
H_VDALERT_N_VR R329 1 0R04 PAD-2-GP H_VDALERT_N



FDI

20 DL_FSYNC_0
20 DL_LSYNC_0
20 DL_FSYNC_1
20 DL_LSYNC_1
20 FDI_INT

20 FDI_TX_DP[0..7]
20 FDI_TX_DN[0..7]

PCIEX16

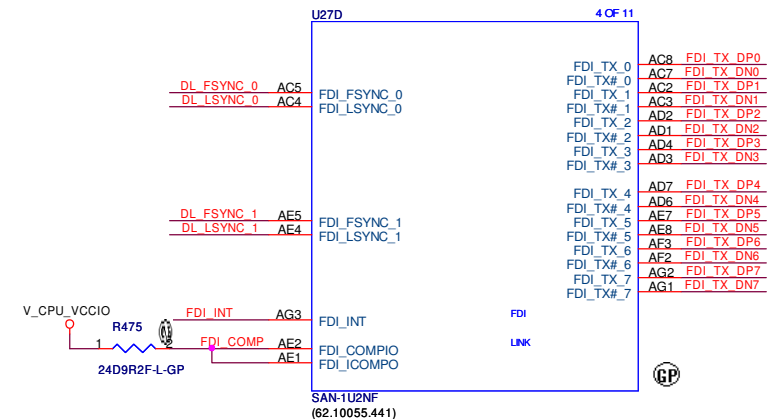
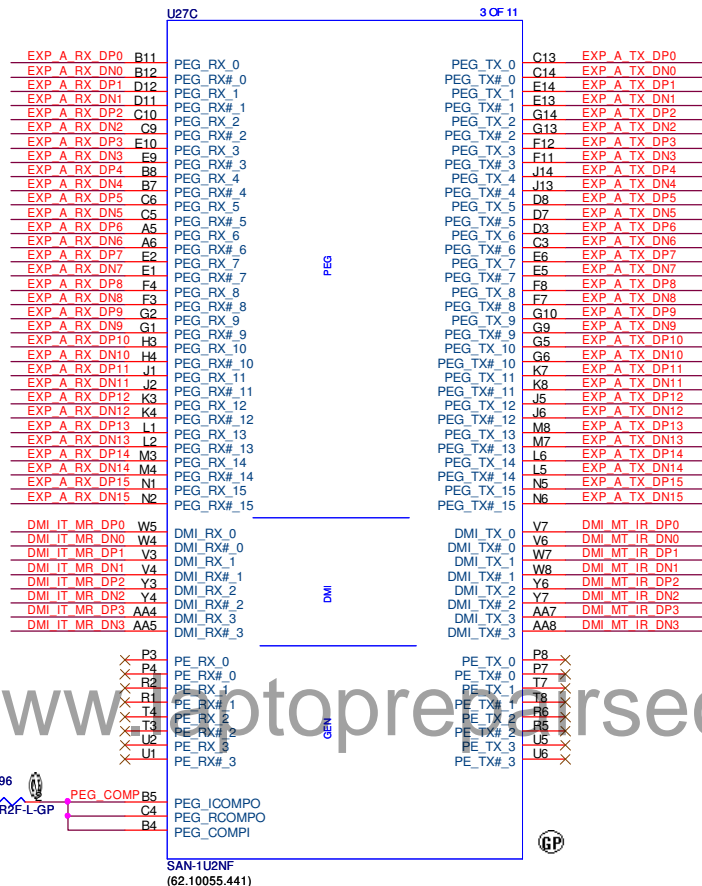
26 EXP_A_TX_DP[0..15]
26 EXP_A_TX_DN[0..15]

26 EXP_A_RX_DP[0..15]
26 EXP_A_RX_DN[0..15]

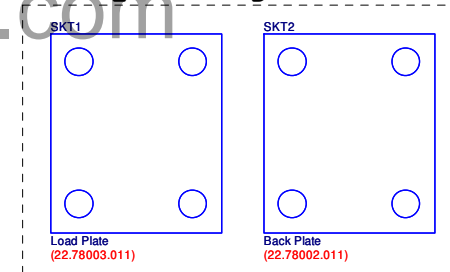
DMI

22 DMI_IT_MR_DP[0..3]
22 DMI_IT_MR_DN[0..3]

22 DMI_MT_IR_DP[0..3]
22 DMI_MT_IR_DN[0..3]



Sandy Bridge Socket



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DDR DATA

15 M_DATA_A[0..63]
17 M_DATA_B[0..63]
15 M_DQS_A_DP[0..8]
16 M_DQS_A_DN[0..8]
17 M_DQS_B_DP[0..8]
17 M_DQS_B_DN[0..8]

15 M_DATA_A_CB[0..7]
17 M_DATA_B_CB[0..7]

DDR CMD/ADD

15 M_MAA_A[0..15]
17 M_MAA_B[0..15]
15 M_WE_A_N
15 M_CAS_A_N
15 M_RAS_A_N
15 M_SBS_A0
15 M_SBS_A1
15 M_SBS_A2

17 M_WE_B_N
17 M_CAS_B_N
17 M_RAS_B_N
17 M_SBS_B0
17 M_SBS_B1
17 M_SBS_B2

DDR CTRL

15 M_SCS_A_N0
15 M_SCS_A_N1
15 M_SCKE_A0
15 M_SCKE_A1
15 M_SCKE_B0
15 M_SCKE_B1
15 M_ODT_A0
15 M_ODT_A1

17 M_SCS_B_N0
17 M_SCS_B_N1
17 M_SCKE_B0
17 M_SCKE_B1
17 M_ODT_B0
17 M_ODT_B1

DDR CLOCK

15 CK_M_DDR0_A_DP
15 CK_M_DDR0_A_DN
15 CK_M_DDR1_A_DP
15 CK_M_DDR1_A_DN

17 CK_M_DDR0_B_DP
17 CK_M_DDR0_B_DN
17 CK_M_DDR1_B_DP
17 CK_M_DDR1_B_DN

DDR OTHERS

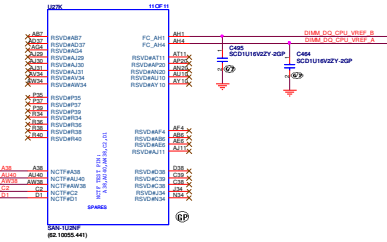
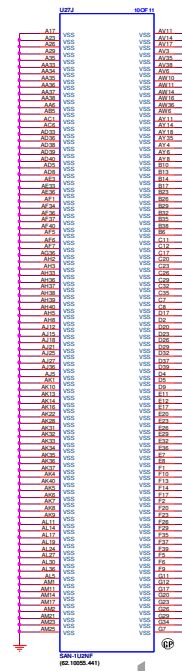
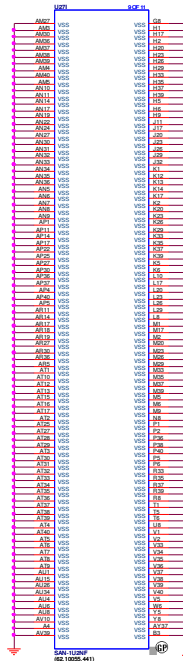
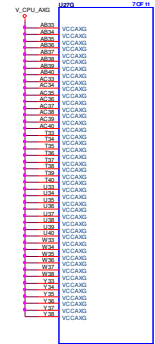
15,17 DDR3_DRAMRST_N

U27A

1 OF 11

M_MAA_A0_AV27	SA_MA_0	SA_MA_0	A0	M_DATA_A0
M_MAA_A1_AV24	SA_MA_1	SA_MA_1	A1	M_DATA_A1
M_MAA_A2_AW24	SA_MA_2	SA_MA_2	A2	M_DATA_A2
M_MAA_A3_AW23	SA_MA_3	SA_MA_3	A3	M_DATA_A3
M_MAA_A4_AV23	SA_MA_4	SA_MA_4	A4	M_DATA_A4
M_MAA_A5_AT24	SA_MA_5	SA_MA_5	A5	M_DATA_A5
M_MAA_A6_AT23	SA_MA_6	SA_MA_6	A6	M_DATA_A6
M_MAA_A7_AL22	SA_MA_7	SA_MA_7	A7	M_DATA_A7
M_MAA_A8_AV22	SA_MA_8	SA_MA_8	A8	M_DATA_A8
M_MAA_A9_AT22	SA_MA_9	SA_MA_9	A9	M_DATA_A9
M_MAA_A10_AV28	SA_MA_10	SA_MA_10	A10	M_DATA_A10
M_MAA_A11_AL21	SA_MA_11	SA_MA_11	A11	M_DATA_A11
M_MAA_A12_AT21	SA_MA_12	SA_MA_12	A12	M_DATA_A12
M_MAA_A13_AW22	SA_MA_13	SA_MA_13	A13	M_DATA_A13
M_MAA_A14_AL20	SA_MA_14	SA_MA_14	A14	M_DATA_A14
M_MAA_A15_AT20	SA_MA_15	SA_MA_15	A15	M_DATA_A15
M_WE_A_N_AW23	SA_WE#	SA_WE#	A17	M_DATA_A17
M_CAS_A_N_AV20	SA_CAS#	SA_CAS#	A18	M_DATA_A18
M_RAS_A_N_AL23	SA_RAS#	SA_RAS#	A19	M_DATA_A19
M_SBS_A0_AV29	SA_BS_0	SA_BS_0	A21	M_DATA_A21
M_SBS_A1_AW28	SA_BS_1	SA_BS_1	A22	M_DATA_A22
M_SBS_A2_AV20	SA_BS_2	SA_BS_2	A23	M_DATA_A23
M_SCS_A_N0_AL29	SA_CSF_0	SA_CSF_0	A26	M_DATA_A26
M_SCS_A_N1_AW30	SA_CSF_1	SA_CSF_1	A27	M_DATA_A27
M_SCKE_A0_AV19	SA_CKE_0	SA_CKE_0	A31	M_DATA_A31
M_SCKE_A1_AL19	SA_CKE_1	SA_CKE_1	A32	M_DATA_A32
M_SCKE_B0_AV18	SA_CKE_2	SA_CKE_2	A33	M_DATA_A33
M_SCKE_B1_XV18	SA_CKE_3	SA_CKE_3	A34	M_DATA_A34
M_ODT_A0_AV21	SA_ODT_0	SA_ODT_0	A36	M_DATA_A36
M_ODT_A1_AL22	SA_ODT_1	SA_ODT_1	A37	M_DATA_A37
M_ODT_B0_AL20	SA_ODT_2	SA_ODT_2	A38	M_DATA_A38
M_ODT_B1_XW33	SA_ODT_3	SA_ODT_3	A39	M_DATA_A39
CK_M_DDR0_A_DP_AY25	SA_CK_0	SA_CK_0	A44	M_DATA_A44
CK_M_DDR0_A_DN_AW25	SA_CK#_0	SA_CK#_0	A45	M_DATA_A45
CK_M_DDR1_A_DP_AL26	SA_CK_1	SA_CK_1	A46	M_DATA_A46
CK_M_DDR1_A_DN_AW27	SA_CK#_1	SA_CK#_1	A47	M_DATA_A47
M_ODT_A0_AV27	SA_CK_2	SA_CK_2	A48	M_DATA_A48
M_ODT_A1_XV26	SA_CK#_2	SA_CK#_2	A49	M_DATA_A49
M_ODT_B0_XV26	SA_CK_3	SA_CK_3	A50	M_DATA_A50
M_ODT_B1_XV26	SA_CK#_3	SA_CK#_3	A51	M_DATA_A51
DDR3_DRAMRST_N_1_R637	SM_DRAMRST#	SM_DRAMRST#	A52	M_DATA_A52
OR0402-PAD-2-GP			A53	M_DATA_A53
SCDIU10V2KX4GP			A54	M_DATA_A54
			A55	M_DATA_A55
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			A298	M_DATA_A298
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			A301	M_DATA_A301
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			A303	M_DATA_A303
			A304	M_DATA_A304
			A305	M_DATA_A305
			A306	M_DATA_A

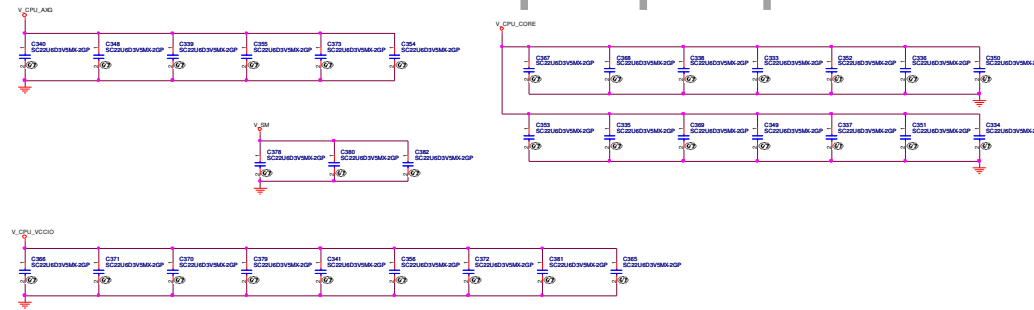
17 DIMM DQ CPU_VREF_B
15 DIMM DQ CPU_VREF_A



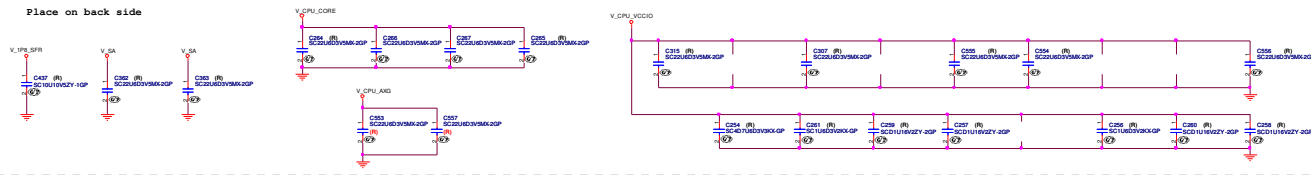
Net	CAP	AMOUNT
Vcore	22uf 0805	14+4
VCCIO	22uf 0805	9+16 (R)
V_AXG	22uf 0805	4+2 (R)
VCCSA	10uf 0805	2+0
VDDQ	22uf 0805	9
VCCPLL	10uf 0805	1

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Place in the CPU Cavity Area



Place on back side



```

10      H_TDO
10      H_TDI
10      H_TMS
10      H_TCK
10      H_TRST_N
10,36   H_CPIRST_N
10      H_FREQ_N
10      H_PRODY_N
10,19   H_PWRGD
10,19,36 PLTRST_N

15,17,36 SMB_DATA_MAIN
15,17,36 SMB_CLK_MAIN

10      XDP_DRESET_N

10      H_BPM0
10      H_BPM1
10      H_BPM2
10      H_BPM3
10      H_BPM4
10      H_BPM5
10      H_BPM6
10      H_BPM7

```

```

19 PCH_JTAG_RST_R
19,35 PCH_DPWR0K
19 PCH_JTAG_TDO
19 PCH_JTAG_TDI
19 PCH_JTAG_TMS
19 PCH_JTAG_TCK
19,45 FP_RST_N
SW_ON_N

19,21,36 PIWRGD_3V
20 CK_XDPG_PCH_100M_DP
20 CK_XDPG_PCH_100M_DIN
22 USB_OC0_R_N
22 USB_OC1_R_N
22 USB_OC2_R_N
22 USB_OC3_R_N
22 USB_OC4_R_N
22 USB_OC5_R_N
22 USB_OC6_R_N

```

19,36 L_AD0 >>>
19,36 L_AD1 >>>
19,36 L_AD2 >>>
19,36 L_AD3 >>>
19,36 L_FRAME_N >>>
20 CK_P_33M_LPCP80 >>>

26,36 PLTRST_SL_N >>>
10 TPEV_SNB_PCUIDEBUG_0 <<<
19,50 VR_READY >>>

Figure 10 illustrates the pinmux configuration for the 12/23 JAKC. The diagram shows a series of multiplexers (R426, R379, R385, R384, R428, R358, R360, R359) routing various signals to different pins. The signals and their destinations are as follows:

- V_CPU_VCCIO** (Input) connects to **R426**, which routes to **H_TDO**.
- Place Near CPU** (Label) connects to **R379**, which routes to **H_TDI**.
- Place Near CPU** (Label) connects to **R385**, which routes to **H_TMS**.
- Place Near CPU** (Label) connects to **R385**, which routes to **H_TCK**.
- Place Any where** (Label) connects to **R384**, which routes to **H_TRST_N**.
- H_CPUST_N** (Input) connects to **R428**, which routes to **H_RSTOUT_XDP_N**.
- VRI_READY** (Input) connects to **R358**, which routes to **XDP_VRI_READY**.
- 12/23 JAKC** (Connector) is highlighted with a red oval.
- V_CPU_VCCIO** (Input) connects to **R360**, which routes to **XDP_EAR**.
- XDP_EAR** (Input) connects to **R359**, which routes to **TPEV_SNB_PCLKDEBUG_0**.

~~All parts can be placed at back side~~

ional signals

V_CPU_VCC0

V_CPU_VCC1

XDP CPU1

12/23 JACK

0V SMC CONNECTION

12V

CK 100M CPU_XDP_DN

CK 100M CPU_XDP_DP

CK_XDP_S_DN

CK_XDP_S_DP

TPAD28 TP6

TPAD28 TP5

TPAD28 TP4

TPAD28 TP3

TPAD28 TP2

TPAD28 TP1

TPAD28 TP0

TPAD28 TP7

TPAD28 TP8

TPAD28 TP9

TPAD28 TP10

TPAD28 TP11

TPAD28 TP12

TPAD28 TP13

TPAD28 TP14

TPAD28 TP15

TPAD28 TP16

TPAD28 TP17

TPAD28 TP18

TPAD28 TP19

TPAD28 TP20

TPAD28 TP21

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TPAD28 TP215

TPAD28 TP216

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TPAD28 TP245

TPAD28 TP246

TPAD28 TP247

TPAD28 TP248

TPAD28 TP249

TPAD28 TP250

TPAD28 TP251

TPAD28 TP252

TPAD28 TP253

TPAD28 TP254

TPAD28 TP255

All parts can be placed at back side

[illegible]

Pin height 2.3mm

Follow Eagle

<Variant Name>



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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

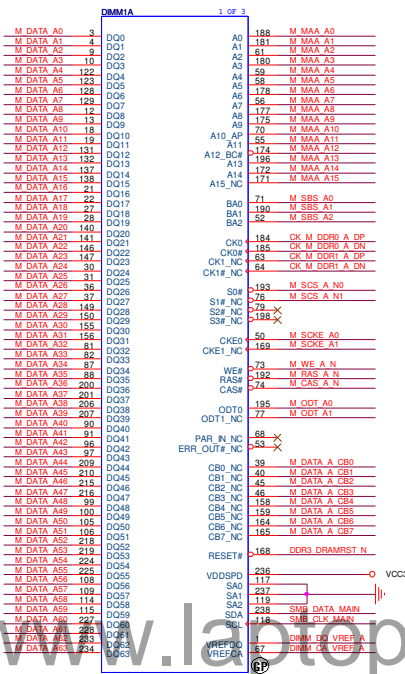
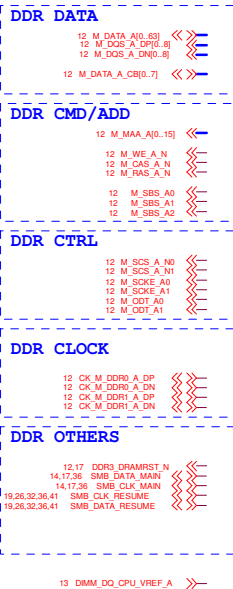
Title

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Document Number	Rosa_Mission_Hills
-----------------	--------------------

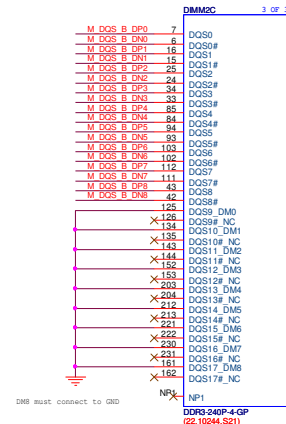
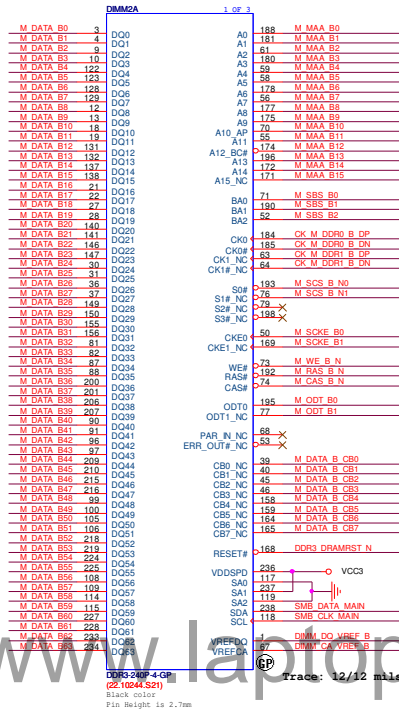
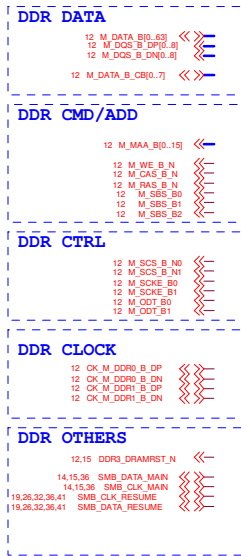
Date: Sunday, March 20, 2011

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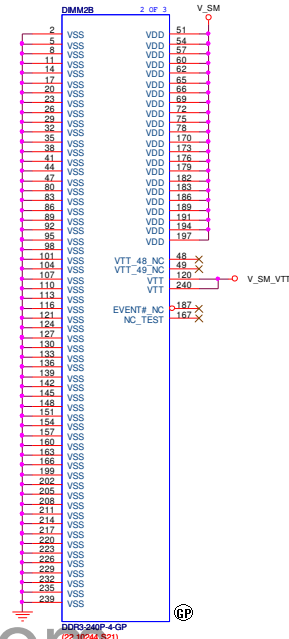
Remove Channel A, DIMM1

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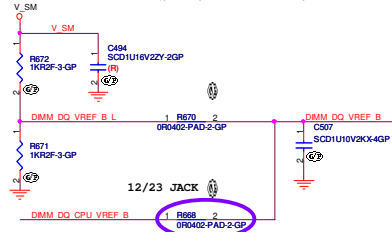


CHANNEL B DIMM1

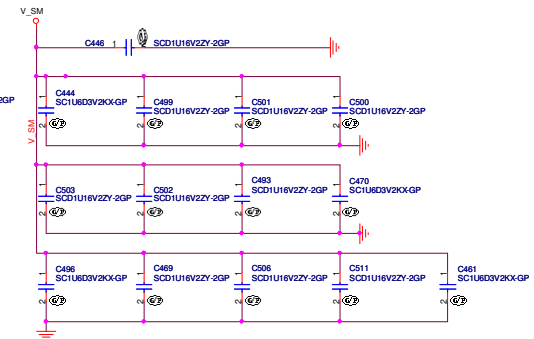
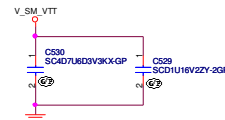
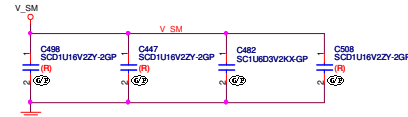
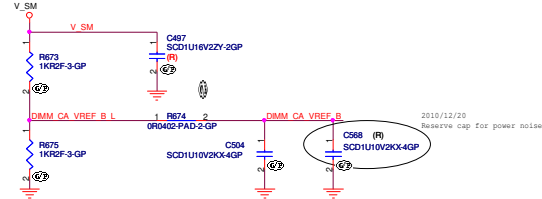
SMB ADDRESS: 010
SPD R/W: 0'A5, 0'A4



DIMM VREF DQ B (To DIMM/CPU)



DIMM VREF CA B (To DIMM)



<Variant Name>

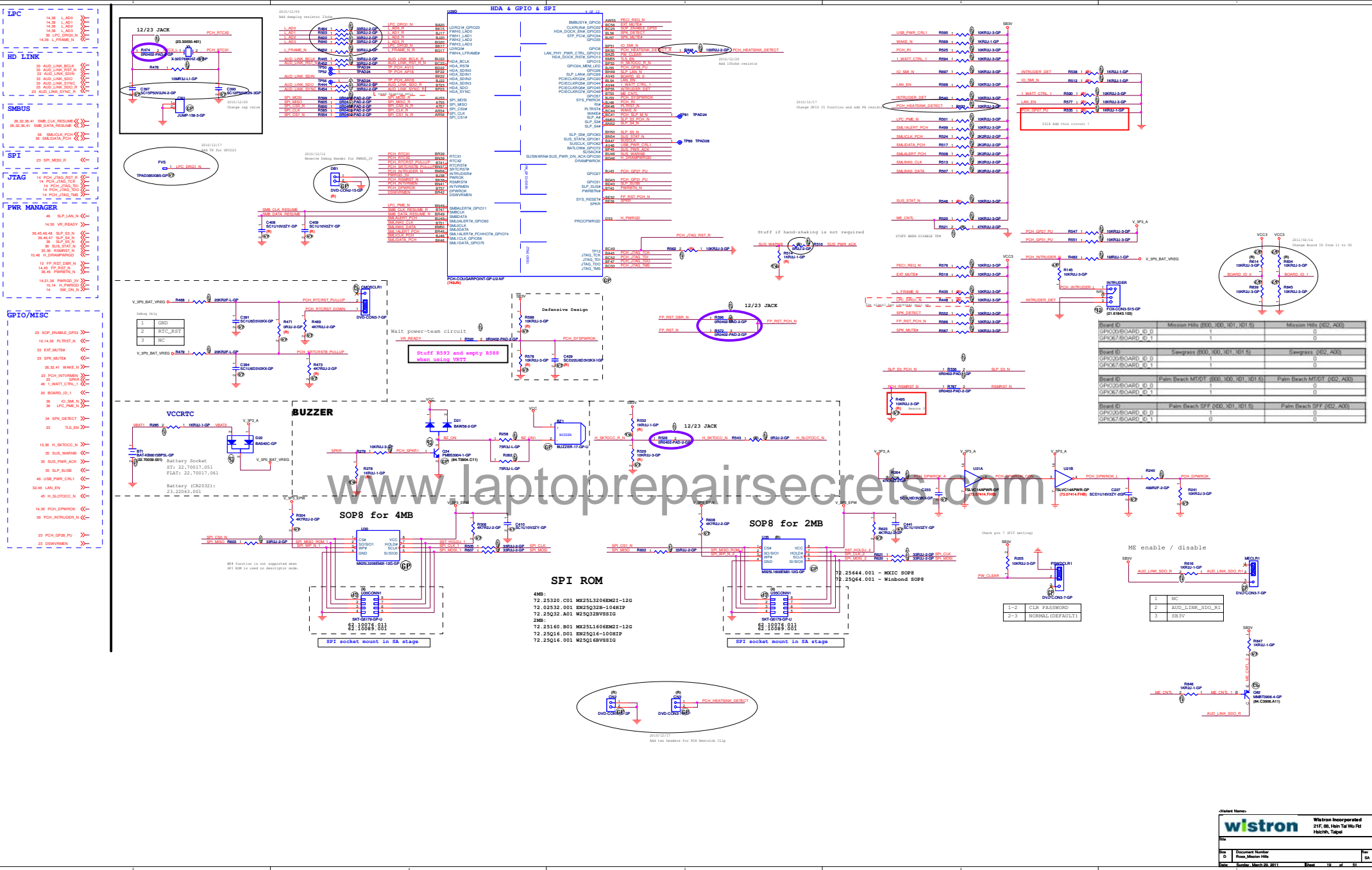
wistron

Wistron Incorporated
21F, 88, Hei Tai Wu Rd
Hsichih, Taipei

Title		
Size	Document Number	Rev
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Remove Channel B, DIMM1

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CPU CLOCK

14 CK_100M_CPU_XDP_DN
14 CK_100M_CPU_XDP_DP

PCI CLOCK

36 CK_P_33M_SIO
32 CK_PCH_33M_FB
14 CK_P_33M_LPCFB

PCIE CLOCK

26 CK_PE_100M_16PORT_DP
26 CK_PE_100M_16PORT_DN
10 CK_PE_100M_MCP_DN
10 CK_PE_100M_MCP_DP

14 CK_XDP_PCH_100M_DP
14 CK_XDP_PCH_100M_DN

41 CK_PCE_1PCIE1_DN
41 CK_PCE_1PCIE1_DP

41 CK_PCE_2PCIE1_DN
41 CK_PCE_2PCIE1_DP

41 CK_PCE_3PCIE1_DN
41 CK_PCE_3PCIE1_DP

32 CK_GLAN_DN
32 CK_GLAN_DP

14M CLOCK

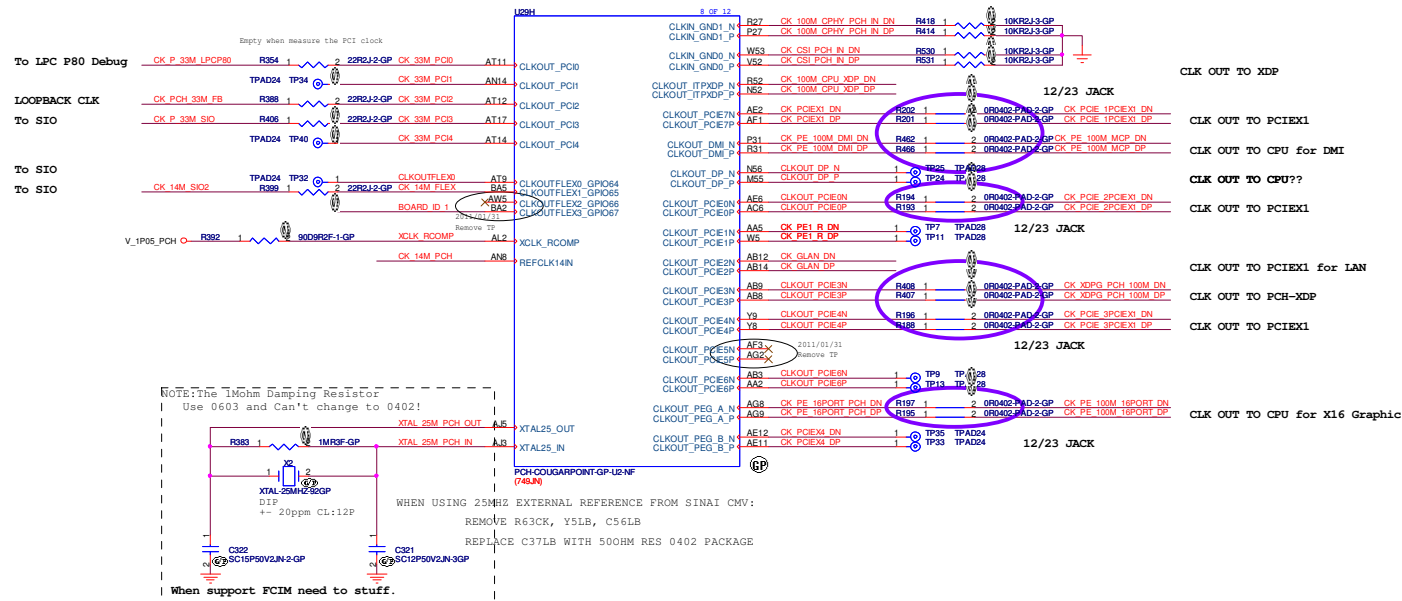
9 CK_14M_PCH
36 CK_14M_SIO2
19 BOARD_ID_1

FDI

11 FDI_TX_DN(0.7)
11 FDI_TX_DP(0.7)
11 DL_FSYNC_0
11 DL_FSYNC_1
11 DL_FSYNC_2
11 FDI_INT

NVRAM

23 NVR_CLE





PCI

20 CK_PCH_33M_FB
23 P_GNT_N0
23 P_GNT_N1
23 P_GNT_N2
23 P_GNT_N3

DMI

11 DMI_MT_IR_DN0..3
11 DMI_MT_IR_DP0..3
11 DMI_IT_MR_DN0..3
11 DMI_IT_MR_DP0..3
9 100M DMI_PCH_DN
9 100M DMI_PCH_DP

PCIE

32 HSI_LAN_DN1
32 HSI_LAN_DP1
32 HSO_C_LAN_DN1
32 HSO_C_LAN_DP1

41 HSI_DN2
41 HSI_DP2
41 HSO_C_DN2
41 HSO_C_DP2

41 HSI_DN3
41 HSI_DP3
41 HSO_C_DN3
41 HSO_C_DP3

41 HSI_DN4
41 HSI_DP4
41 HSO_C_DN4
41 HSO_C_DP4

USB

30 USB_PCH_DN0
30 USB_PCH_DP0
30 USB_PCH_DN1
30 USB_PCH_DP1
30 USB_PCH_DN2
30 USB_PCH_DP2
30 USB_PCH_DN3
30 USB_PCH_DP3

31 USB_PCH_DN4
31 USB_PCH_DP4
31 USB_PCH_DN5
31 USB_PCH_DP5

31 USB_PCH_DN6
31 USB_PCH_DP6
31 USB_PCH_DN7
31 USB_PCH_DP7

31 USB_PCH_DN8
31 USB_PCH_DP8
31 USB_PCH_DN9
31 USB_PCH_DP9

31 USB_PCH_DN10
31 USB_PCH_DP10
31 USB_PCH_DN11
31 USB_PCH_DP11

30 USB_OC_01*
30 USB_OC_23*

31 USB_OC_1011*
31 USB_OC_89*
31 USB_OC_45*

VGA CLK

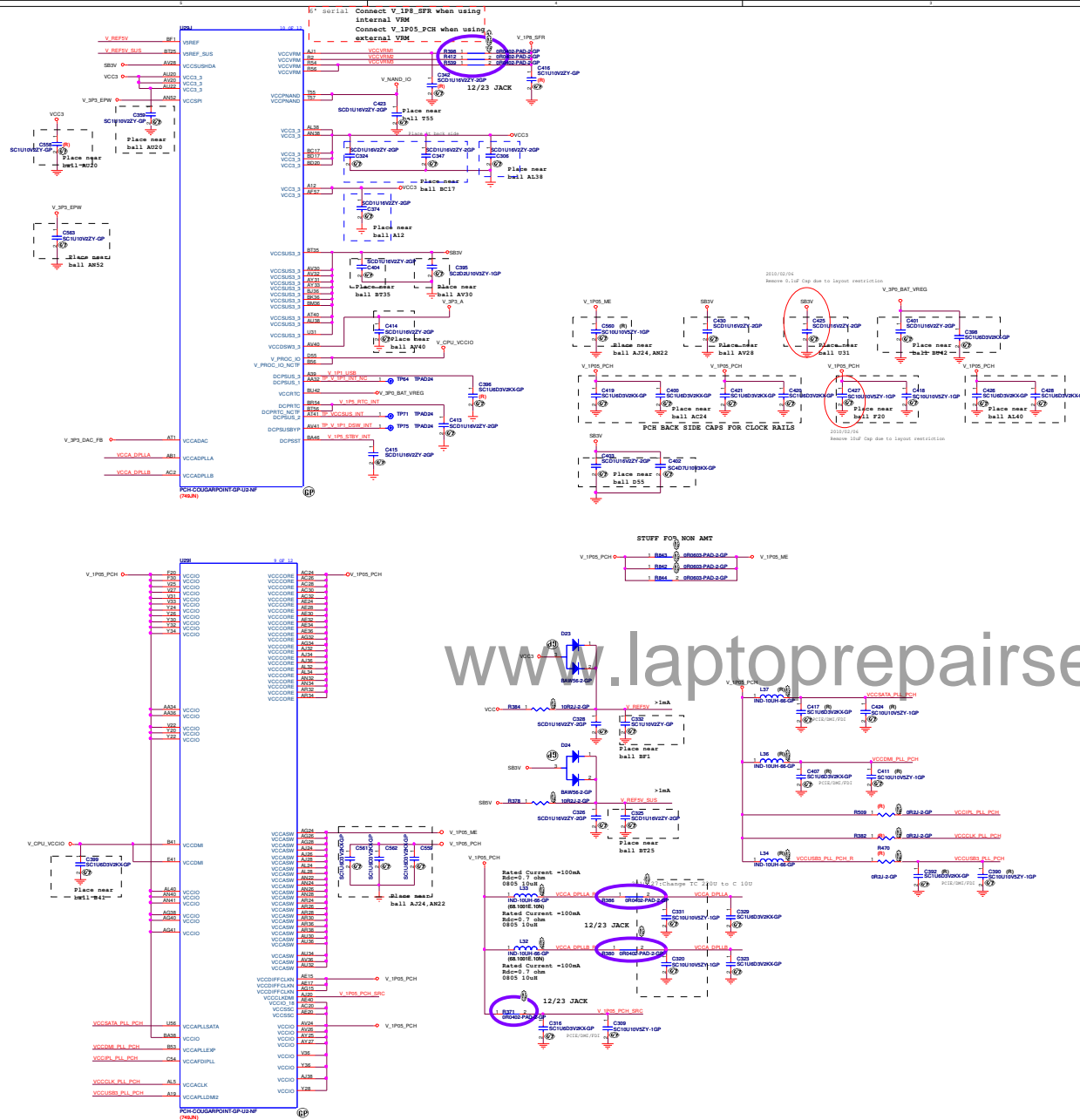
9 CK_96M_DREF_DN
9 CK_96M_DREF_DP

OTHERS

14 USB_OC0_R_N
14 USB_OC0_R_P
14 USB_OC0_R_N
14 USB_OC0_R_P
14 USB_OC0_R_N
14 USB_OC0_R_P
14 USB_OC0_R_N
14 USB_OC0_R_P

PCI

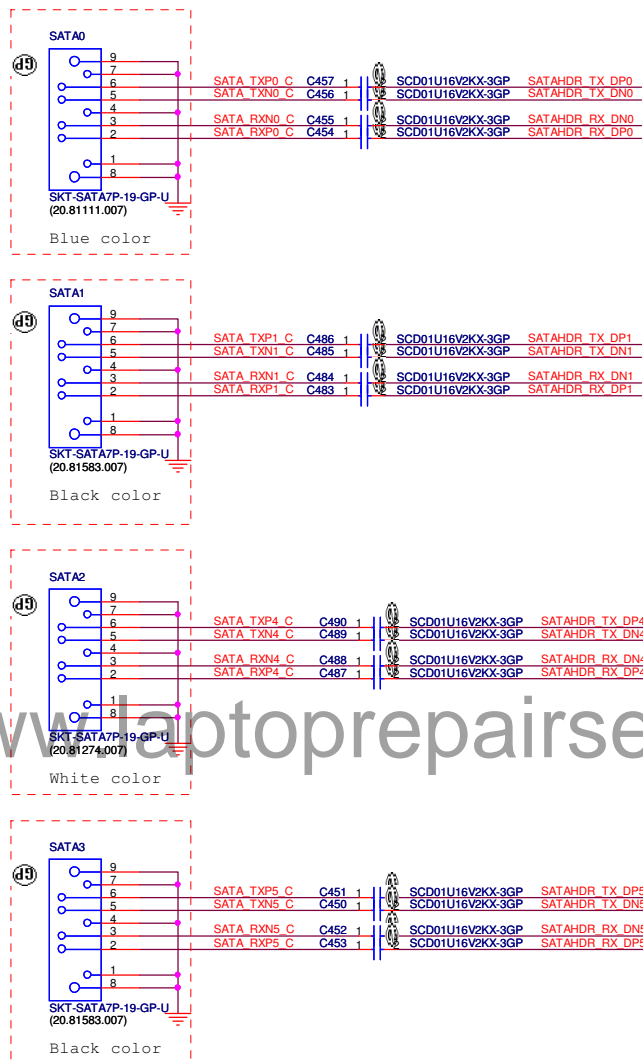
TPAD24 TP31 1 TP_BH# B18#
TPAD24 TP36 1 CK_PCH_33M_FB B015#
TPAD24 TP45 1 P_PERR# N_B06#
TPAD24 TP45 1 P_STOP# N_B012#
TPAD24 TP45 1 P_PLOCK# N_B012#
TPAD24 TP45 1 P_TRDY# N_B08#
TPAD24 TP45 1 P_PERR# N_B03#
TPAD24 TP45 1 P_FRAME# N_B011#
P_GNT_N0 B015#
P_GNT_N1 A08#
P_GNT_N2 B012#
P_GNT_N3 B02#
P_REQ_N0 B05#
P_REQ_N1 B15#
P_REQ_N2 B09#
P_REQ_N3 A011#
P_INTA_N B010#
P_INTB_N B05#
P_INTC_N B05#
P_INTD_N B05#
P_INTE_N B05#
P_INTF_N A08#
P_INTG_N B115#
P_INTH_N B04#
PARI# DEVSEL#
CLKIN# PCIL00PBACK
R0Y#
PME#
SERR#
STOP#
PLOCK#
TRDY#
PERR#
FRAME#
GNT0#
GNT1#_GPIOS1
GNT2#_GPIOS3
GNT3#_GPIOS5
REQ0#
REQ1#_GPIOS0
REQ2#_GPIOS2
REQ3#_GPIOS4
PIROA#
PIROB#
PIROC#
PIROD#
PIROE#_GPIOS2
PIROF#_GPIOS3
PIROG#_GPIOS4
PIROH#_GPIOS5
C_BE0#
C_BE1#
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BT819#
BT820#
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BT825#
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BT830#
BT831#
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BT838#
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BT840#
BT841#
BT842#
BT843#
BT844#
BT845#
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BT903#
BT904#
BT905#
BT906#
BT907#
BT908#
BT909#
BT910#
BT911#
BT912#
BT913#
BT914#
BT915#
BT916#
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BT918#
BT919#
BT920#
BT921#
BT922#
BT923#
BT924#
BT925#
BT926#
BT927#
BT928#
BT929#
BT930#
BT931#
BT932#
BT933#
BT934#
BT935#
BT936#
BT937#
BT938#
BT939#
BT940#
BT941#
BT942#
BT943#
BT944#
BT945#
BT946#
BT947#
BT948#
BT949#
BT950#
BT951#
BT952#
BT953#
BT954#
BT955#
BT956#
BT957#
BT958#
BT959#
BT960#
BT961#
BT962#
BT963#
BT964#
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BT966#
BT967#
BT968#
BT969#
BT970#
BT971#
BT972#
BT973#
BT974#
BT975#
BT976#
BT977#
BT978#
BT979#
BT980#
BT981#
BT982#
BT983#
BT984#
BT985#
BT986#
BT987#
BT988#
BT989#
BT990#
BT991#
BT992#
BT993#
BT994#
BT995#
BT996#
BT997#
BT998#
BT999#
BT1000#
BT1001#
BT1002#
BT1003#
BT1004#
BT1005#
BT1006#
BT1007#
BT1008#
BT1009#
BT1010#
BT1011#
BT1012#
BT1013#
BT1014#
BT1015#
BT1016#
BT1017#
BT1018#
BT1019#
BT1020#
BT1021#
BT1022#
BT1023#
BT1024#
BT1025#
BT1026#
BT1027#
BT1028#
BT1029#
BT1030#
BT1031#
BT1032#
BT1033#
BT1034#
BT1035#
BT1036#
BT1037#
BT1038#
BT1039#
BT1040#
BT1041#
BT1042#
BT1043#
BT1044#
BT1045#
BT1046#
BT1047#
BT1048#
BT1049#
BT1050#
BT1051#
BT1052#
BT1053#
BT1054#
BT1055#
BT1056#
BT1057#
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BT1059#
BT1060#
BT1061#
BT1062#
BT1063#
BT1064#
BT1065#
BT1066#
BT1067#
BT1068#
BT1069#
BT1070#
BT1071#
BT1072#
BT1073#
BT1074#
BT1075#
BT1076#
BT1077#
BT1078#
BT1079#
BT1080#
BT1081#
BT1082#
BT1083#
BT1084#
BT1085#
BT1086#
BT1087#
BT1088#
BT1089#
BT1090#
BT1091#
BT1092#
BT1093#
BT1094#
BT1095#
BT1096#
BT1097#
BT1098#
BT1099#
BT1100#
BT1101#
BT1102#
BT1103#
BT1104#
BT1105#
BT1106#
BT1107#
BT1108#
BT1109#
BT1110#
BT1111#
BT1112#
BT1113#
BT1114#
BT1115#
BT1116#
BT1117#
BT1118#
BT1119#
BT1120#
BT1121#
BT1122#
BT1123#
BT1124#
BT1125#
BT1126#
BT1127#
BT1128#
BT1129#
BT1130#
BT1131#
BT1132#
BT1133#
BT1134#
BT1135#
BT1136#
BT1137#
BT1138#
BT1139#
BT1140#
BT1141#
BT1142#
BT1143#
BT1144#
BT1145#
BT1146#
BT1147#
BT1148#
BT1149#
BT1150#
BT1151#
BT1152#
BT1153#
BT1154#
BT1155#
BT1156#
BT1157#
BT1158#
BT1159#
BT1160#
BT1161#
BT1162#
BT1163#
BT1164#
BT1165#
BT1166#
BT1167#
BT1168#
BT1169#
BT1170#
BT1171#
BT1172#
BT1173#
BT1174#
BT1175#
BT1176#
BT1177#
BT1178#
BT1179#
BT1180#
BT1181#
BT1182#
BT1183#
BT1184#
BT1185#
BT1186#
BT1187#
BT1188#
BT1189#
BT1190#
BT1191#
BT1192#
BT1193#
BT1194#
BT1195#
BT1196#
BT1197#
BT1198#
BT1199#
BT1200#
BT1201#
BT1202#
BT1203#
BT1204#
BT1205#
BT1206#
BT1207#
BT1208#
BT1209#
BT1210#
BT1211#
BT1212#
BT1213#
BT1214#
BT1215#
BT1216#
BT1217#
BT1218#
BT1219#
BT1220#
BT1221#
BT1222#
BT1223#
BT1224#
BT1225#
BT1226#
BT1227#
BT1228#
BT1229#
BT1230#
BT1231#
BT1232#
BT1233#
BT1234#
BT1235#
BT1236#
BT1237#
BT1238#
BT1239#
BT1240#
BT1241#
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SATA

21 SATAHDR_RX_DP0
21 SATAHDR_RX_DN0
21 SATAHDR_TX_DN0
21 SATAHDR_TX_DP0
21 SATAHDR_RX_DP1
21 SATAHDR_RX_DN1
21 SATAHDR_TX_DN1
21 SATAHDR_TX_DP1
21 SATAHDR_RX_DP4
21 SATAHDR_RX_DN4
21 SATAHDR_TX_DN4
21 SATAHDR_TX_DP4
21 SATAHDR_RX_DP5
21 SATAHDR_RX_DN5
21 SATAHDR_TX_DN5
21 SATAHDR_TX_DP5



NOTE:

PCH only port 0&1 support SATA 3.0

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Hsichih, Taipei

Title

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SA

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PCIEX16

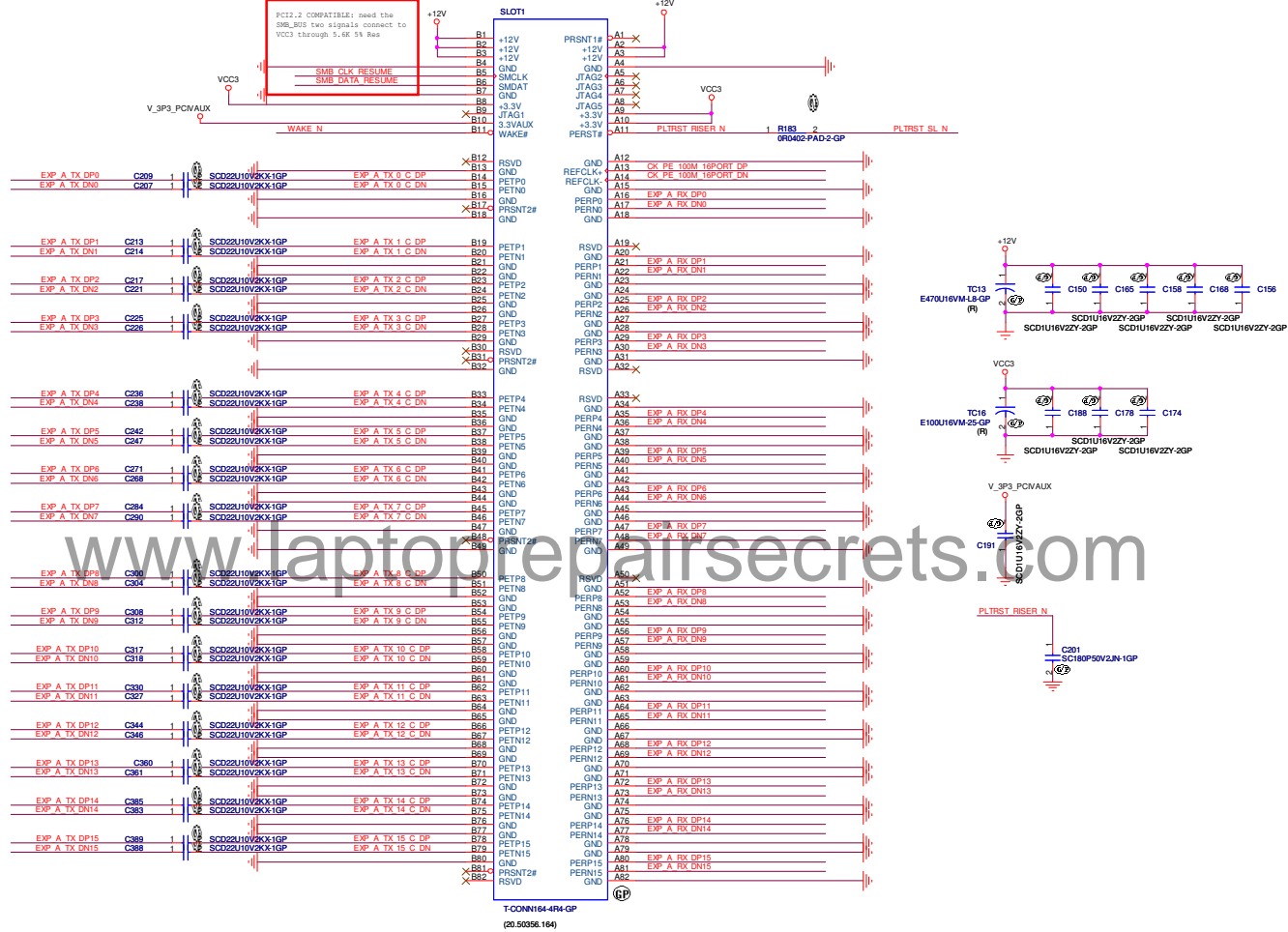
11 EXP_A_RX_DN0..15
11 EXP_A_TX_DP0..15
11 EXP_A_TX_DN0..15
20 CK_PE_100M_16PORT_DP
20 CK_PE_100M_16PORT_DN
14.36 PLTRST_SL_N

OTHERS

19.32.36.41 SMB_CLK_RESUME
19.32.36.41 SMB_DATA_RESUME
19.32.41 WAKE_N

w/o Latch: 20.50352.164
with Latch: 20.50512.164, 20.50356.164

PCIEX16 CONN may need LATCH if supporting 75W GFX Card



<Variant Name>

RGB

21 VGA_RED
21 VGA_GREEN
21 VGA_BLUE

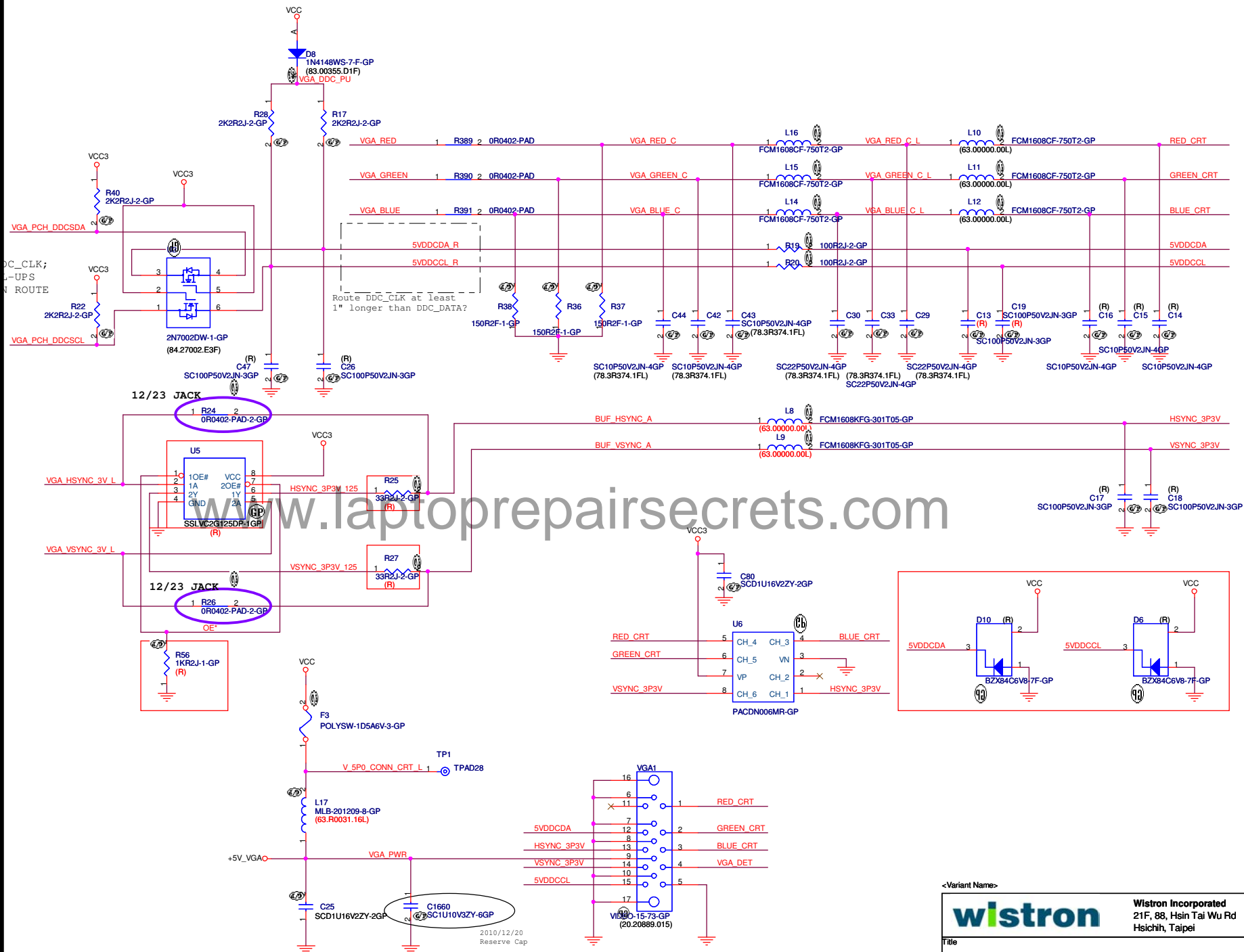
SYNC

21 VGA_HSYNC_3V_L
21 VGA_VSYNC_3V_L

DDC

21 VGA_PCH_DDCSDA
21 VGA_PCH_DDCSCL
21 VGA_DET

DDC_DATA/DDC_CLK;
LOCATE PULL-UPS
ANYWHERE ON ROUTE
OF TRACE



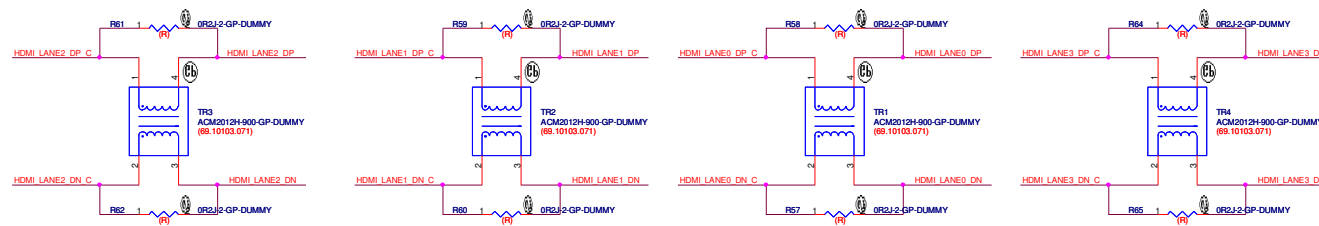
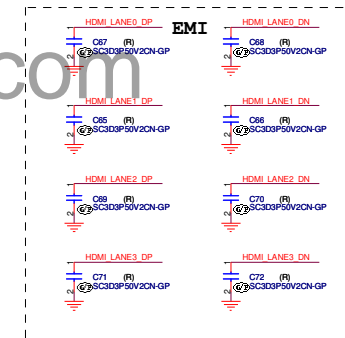
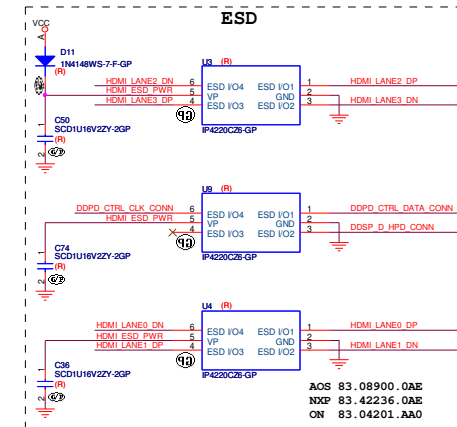
<Variant Name>

wistron			Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title			
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```

21 DDSP_D_TX_DP_0
21 DDSP_D_TX_DN_0
21 DDSP_D_TX_DP_1
21 DDSP_D_TX_DN_1
21 DDSP_D_TX_DP_2
21 DDSP_D_TX_DN_2
21 DDSP_D_TX_DP_3
21 DDSP_D_TX_DN_3
21 DDSP_CTRL_CLK
21 DDSP_CTRL_DATA
21 DDSP_D_HPD

```



DISPLAY PORT

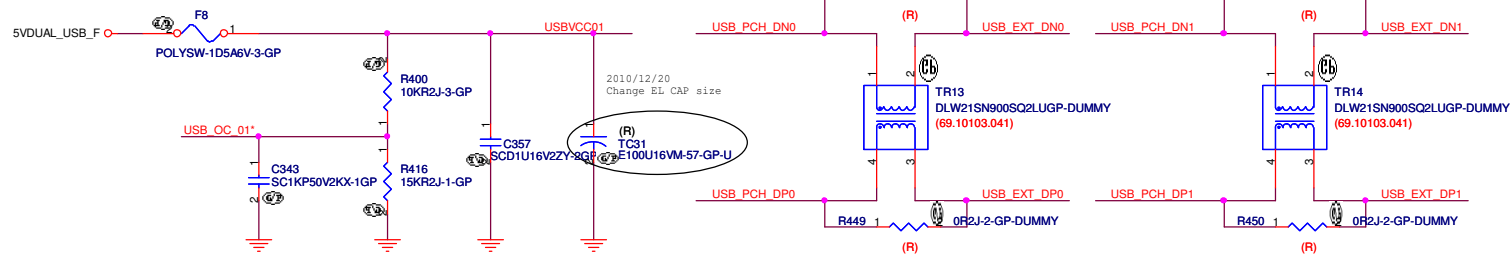
RESERVED

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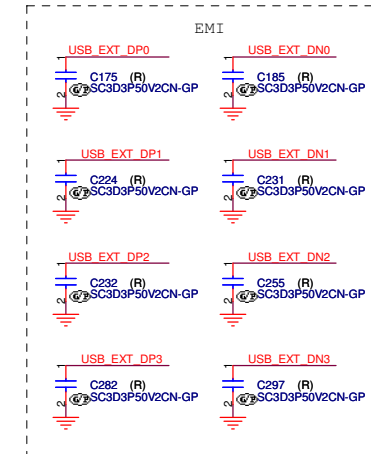
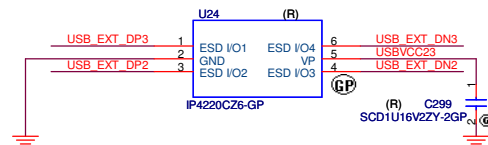
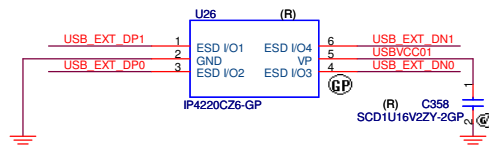
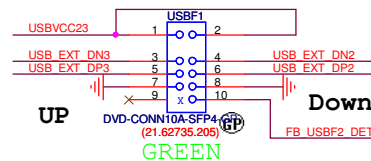
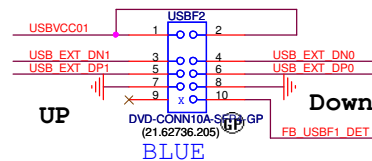
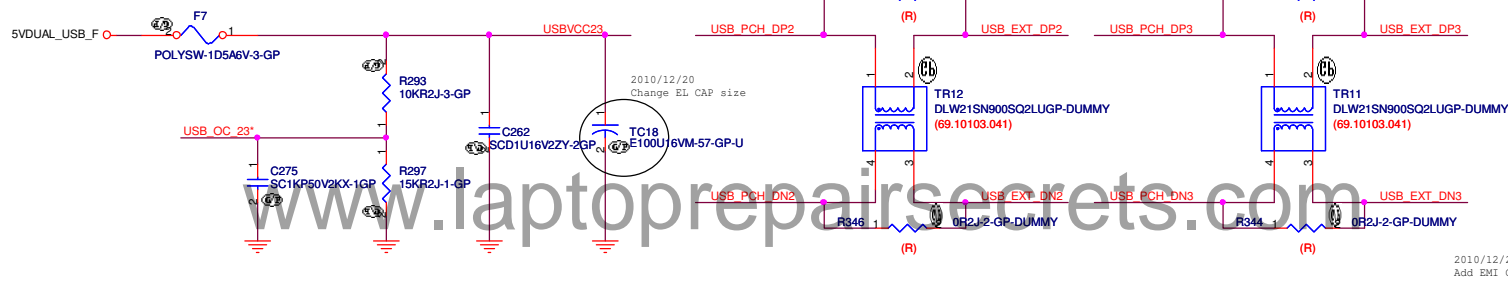
FRONT USB

- 22 USB_PCH_DP0
- 22 USB_PCH_DN0
- 22 USB_PCH_DP1
- 22 USB_PCH_DN1
- 22 USB_OC_01*
- 21 FB_USBF1_DET
- 22 USB_PCH_DP2
- 22 USB_PCH_DN2
- 22 USB_PCH_DP3
- 22 USB_PCH_DN3
- 22 USB_OC_23*
- 21 FB_USBF2_DET
- 22.31 USB_PCH_DN10
- 22.31 USB_PCH_DP10
- 22.31 USB_PCH_DN11
- 22.31 USB_PCH_DP11

FRONT USB PORT



FRONT USB PORT



<Variant Name>

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REAR USB+LAN

```

22 USB_PCH_DP4 <==
22 USB_PCH_DN4 <==
22 USB_PCH_DN5 <==
22 USB_PCH_DPS <==

32 LAN_MDIO2_DP <==
32 LAN_MDIO2_DN <==
32 LAN_MDIO1_DP <==
32 LAN_MDIO1_DN <==
32 LAN_MDIO0_DP <==
32 LAN_MDIO0_DN <==
32 LAN_MDIO3_DP <==
32 LAN_MDIO3_DN <==

32 SPEED_100_N <==
32 SPEED_1000_N <==

```

REAR USB

```

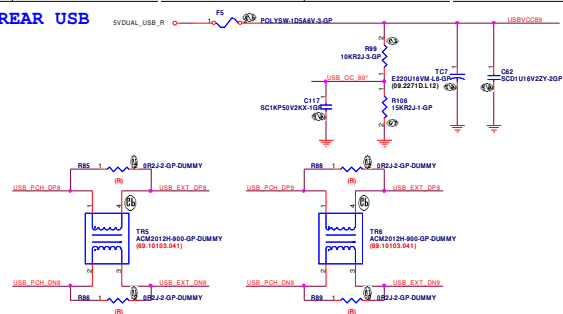
22 USB_PCH_DP8
22 USB_PCH_DP8
22 USB_PCH_DP9
22 USB_PCH_DP9

22 USB_PCH_DP10
22 USB_PCH_DP10
22 USB_PCH_DP11
22 USB_PCH_DP11

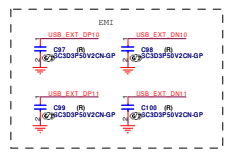
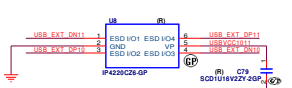
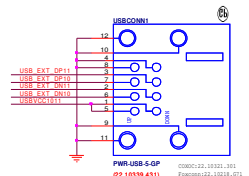
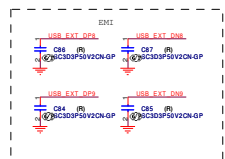
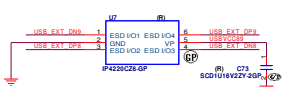
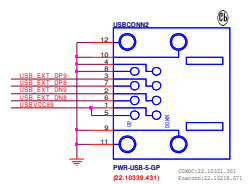
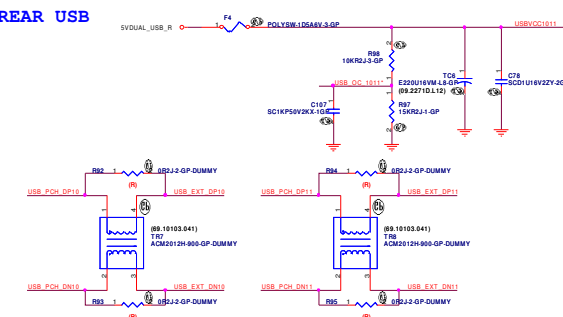
22 USB_OC_89*
22 USB_OC_45*
22 USB_OC_1011*

```

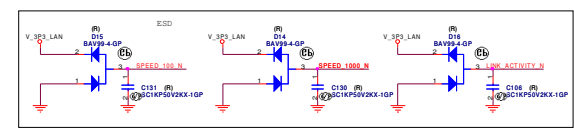
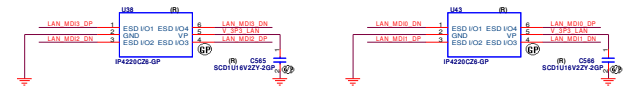
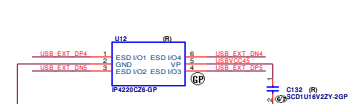
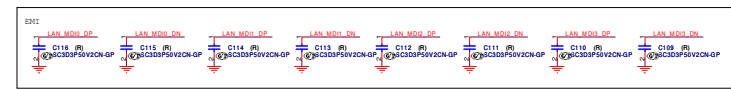
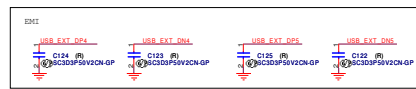
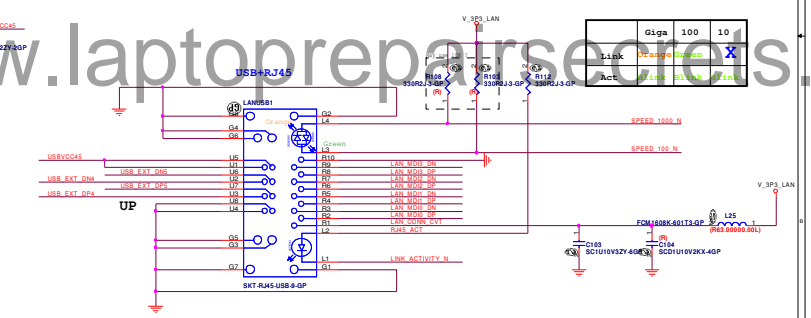
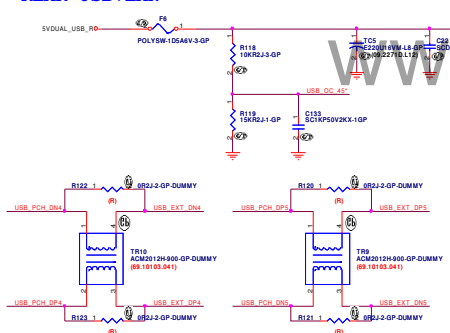
REAR USB



REAR USB



REAR USB+LAN



	Giga	100	10
Link	Orange	Green	X
Act	Blink	Blink	Blink

HD_LINK

19 AUD_LINK_SDN
19 AUD_LINK_SDO
19 AUD_LINK_RST_N
19 AUD_LINK_SYNC
19 AUD_LINK_BCLK

Rear I/O

LINE-OUT
34 LOUT_R
34 LOUT_L
34 LOUT_ID

LINE-IN
34 LIN_R
34 LIN_L
34 LIN_ID

MIC-IN
34 MIC_IN_R
34 MIC_IN_L
34 MIC_ID
34 MIC1_VREF0

Front I/O

HP-OUT
34 FP_OUT_L
34 FP_OUT_R
34 LINE2_ID

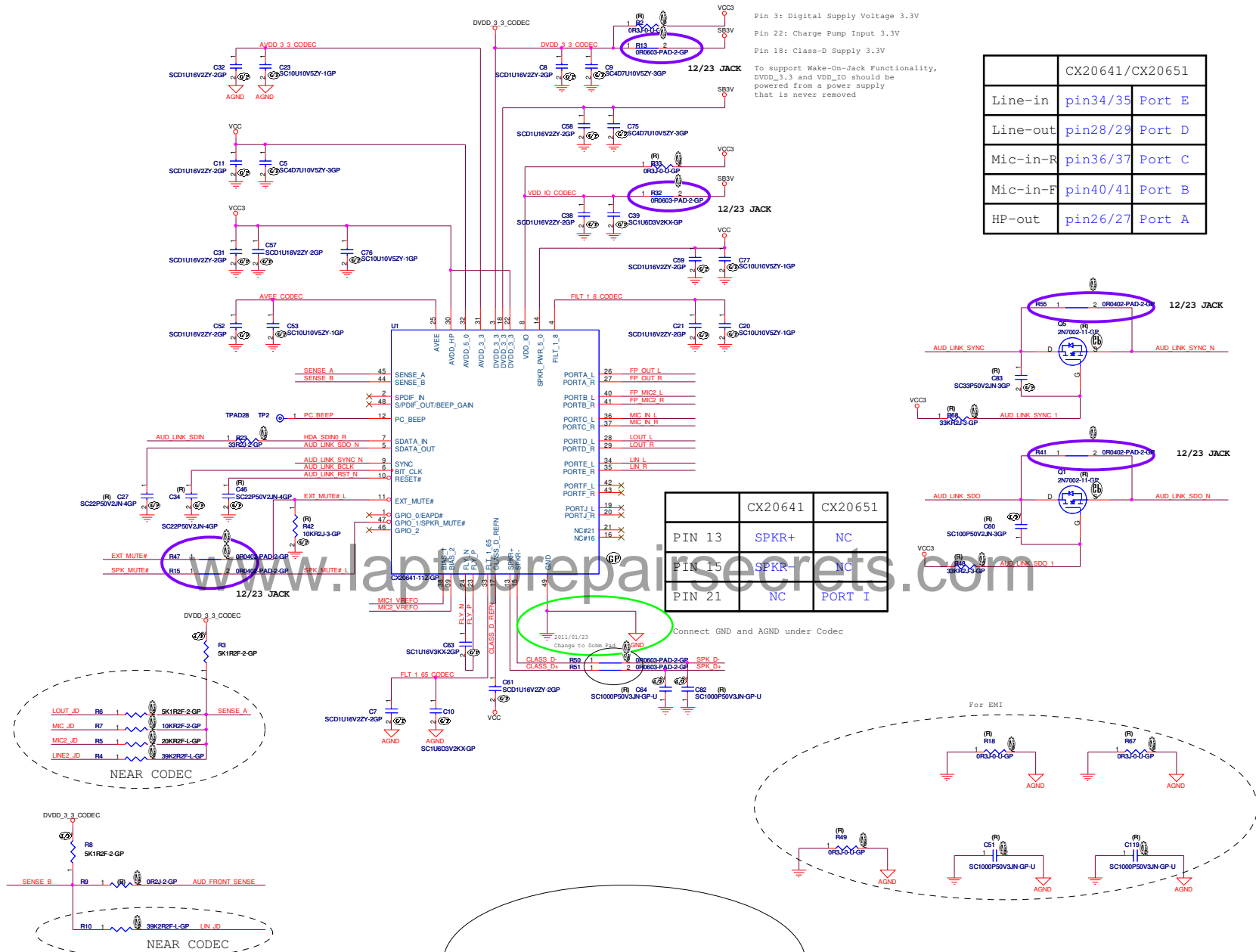
MIC-IN
34 FP_MIC2_R
34 FP_MIC2_L
34 MIC2_ID
34 MIC2_VREF0

Internal Speaker

34 SPK_D-
34 SPK_D+

Others

34 AUD_FRONT_SENSE
19 EXT_MUTE#
19 SPK_MUTE#



Pin 3: Digital Supply Voltage 3.3V
Pin 22: Charge Pump Input 3.3V
Pin 18: Class-D Supply 3.3V
To support Wake-On-Jack Functionality, DVDD_3.3 and VDD_IO should be powered from a power supply that is never removed

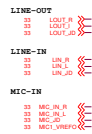
	CX20641/CX20651
Line-in	pin34/35 Port E
Line-out	pin28/29 Port D
Mic-in-R	pin36/37 Port C
Mic-in-F	pin40/41 Port B
HP-out	pin26/27 Port A

	CX20641	CX20651
PIN 13	SPKR+	NC
PIN 15	SPKR-	NC
PIN 21	NC	PORT I

Connect GND and AGND under Codec

Remove De-Pop Circuit

Rear I/O



Front I/O



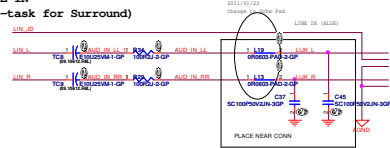
SPEAKER



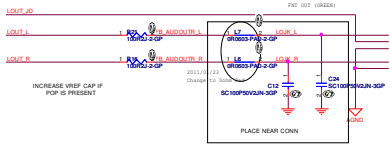
Others



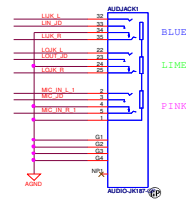
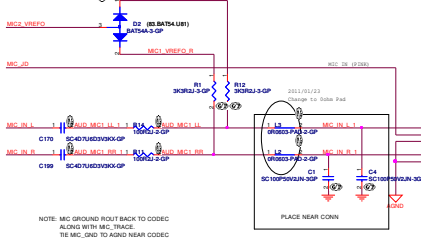
LINE-IN (Re-task for Surround)



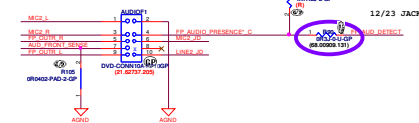
LINE-OUT



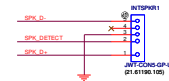
MIC-IN (Re-task for C/LFE)



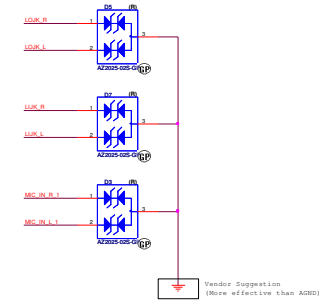
Front Panel



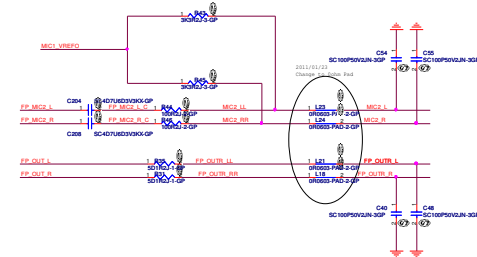
Internal Speaker



ESD

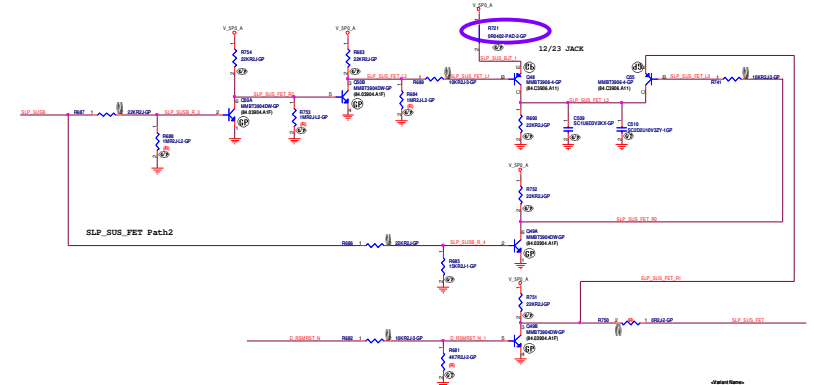
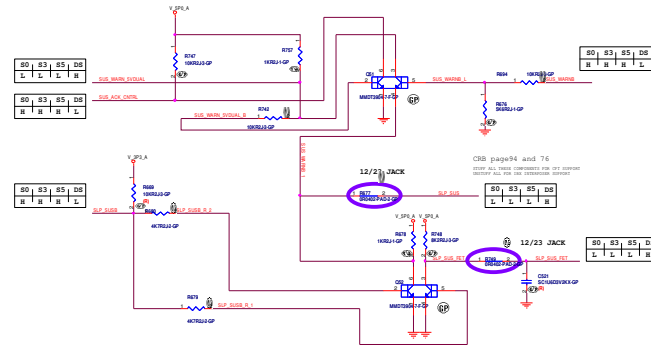
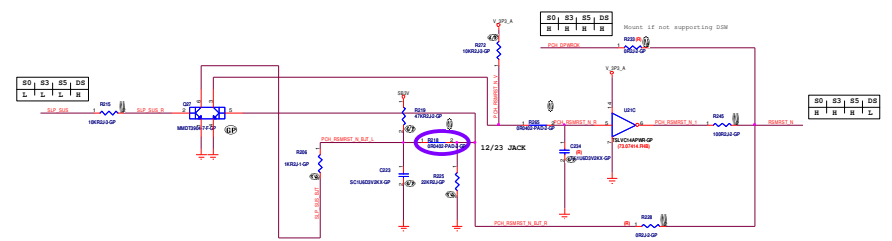
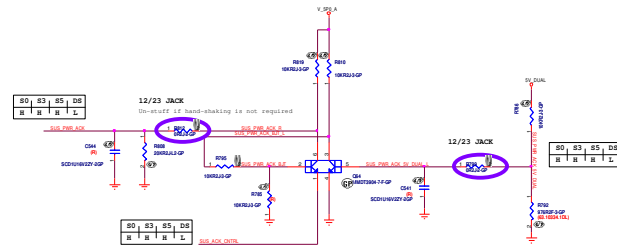


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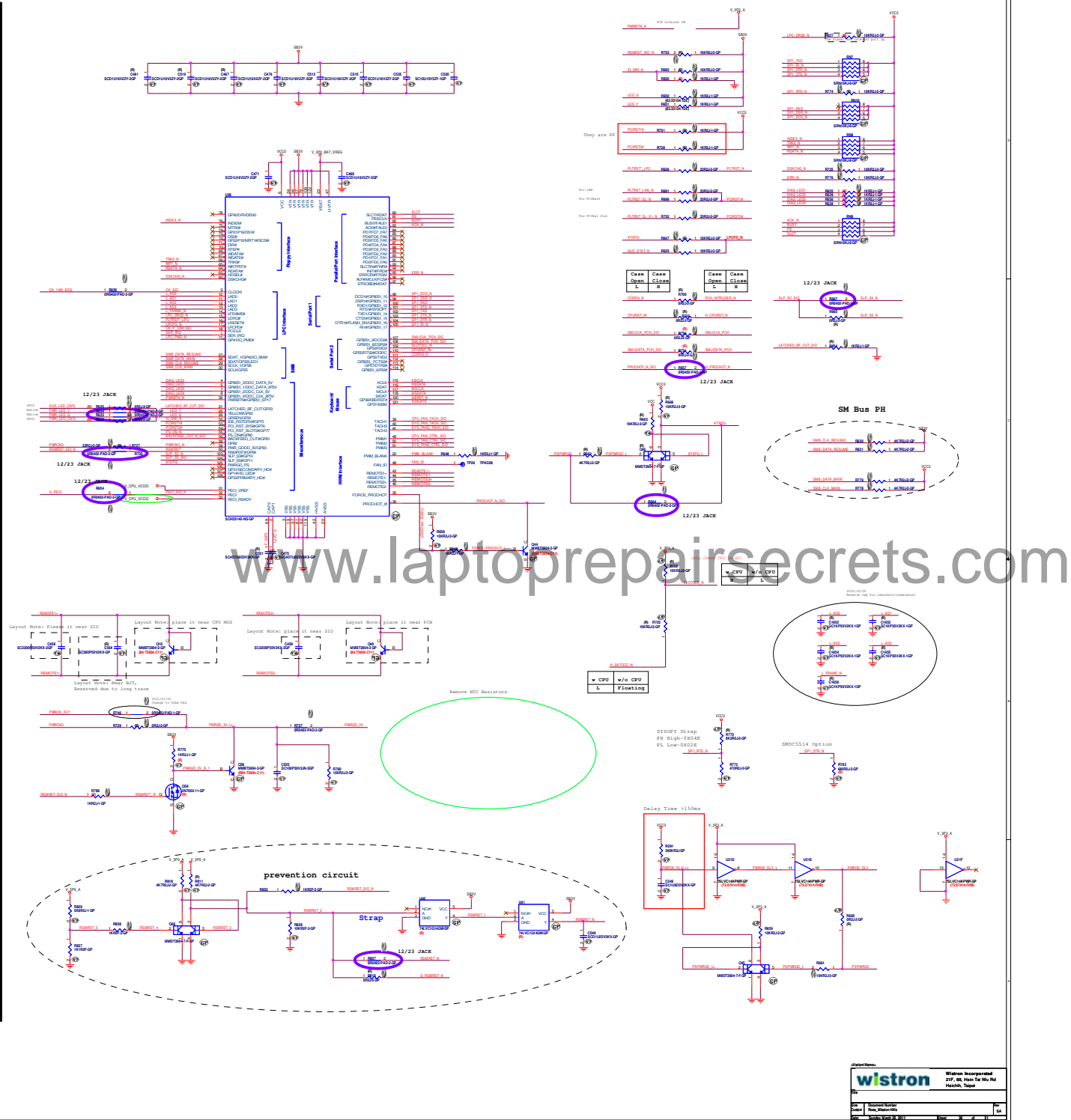


Remove Mute Circuit

10 SUS_PWD_ACK
 10 SUS_WAKE
 14 SUS_WAKE
 48 SUS_WAKE_FET
 48 SUS_WAKE_FET
 14.5 SUS_WAKE_FET
 14.5 SUS_WAKE_FET
 14.5 SUS_WAKE_FET



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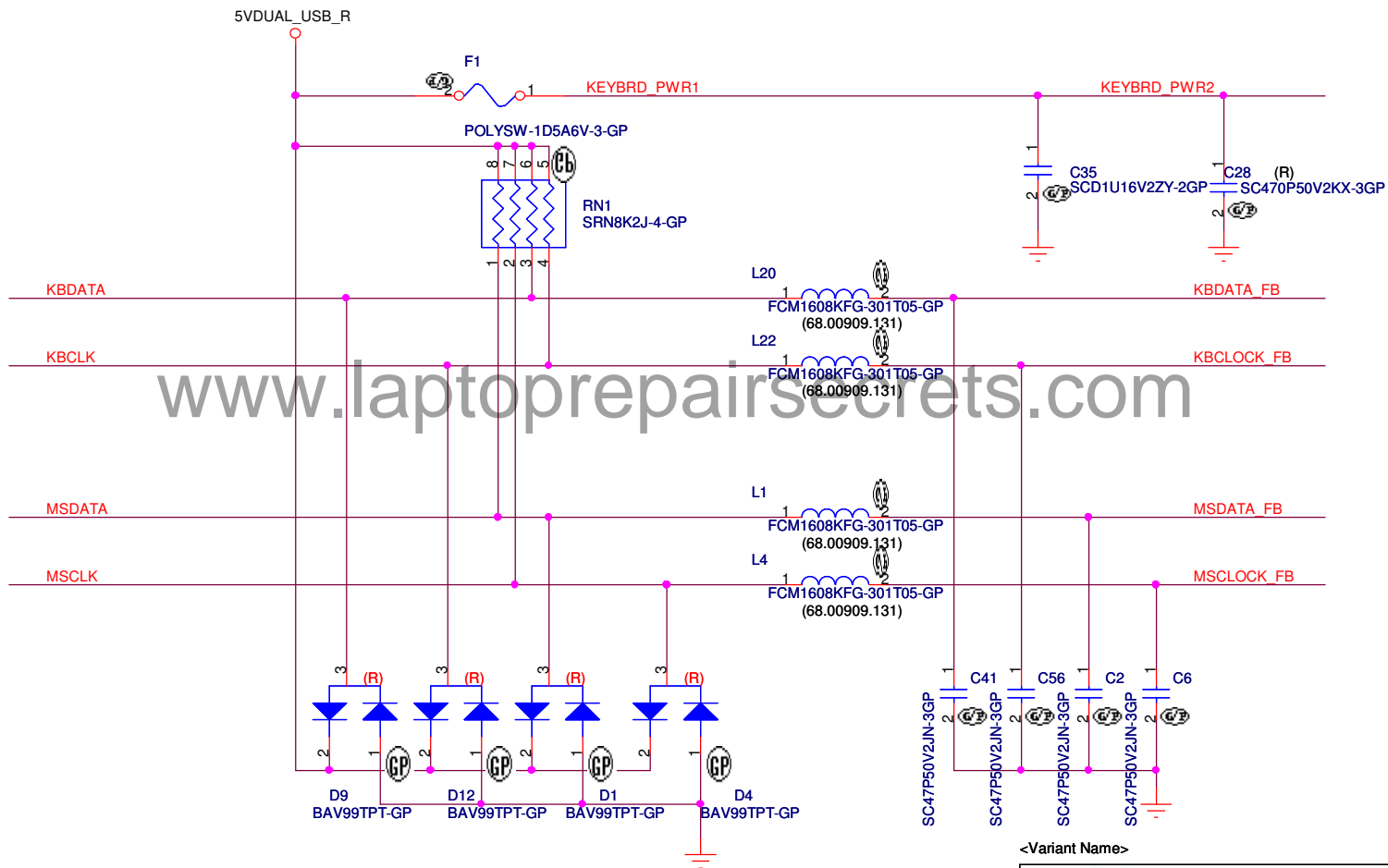


PS2 KB/MS

36 KBDATA <<>>
 36 KBCLK <<>>
 36 MSDATA <<>>
 36 MSCLK <<>>

38 KBDATA_FB <<>>
 38 KBCLOCK_FB <<>>
 38 MSDATA_FB <<>>
 38 MSCLOCK_FB <<>>

38 KEYBRD_PWR2 <<>>



<Variant Name>

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2

1

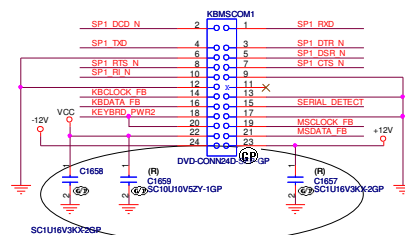
COM Port

36 SP1_RTS_N <<<
 36 SP1_DTR_N <<<
 36 SP1_DSR_N <<<
 36 SP1_RXD <<<
 36 SP1_DCD_N <<<
 36 SP1_TXD <<<
 36 SP1_CTS_N <<<
 36 SP1_RL_N <<<

21 SERIAL_DETECT <<<

KB/MS

37 KBDATA_FB <<<
 37 KBCLK_FB <<<
 37 MSCLK_FB <<<
 37 MSCLK_FB <<<
 37 KEYBRD_PWR2 >>>



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<Variant Name>

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 Hsichih, Taipei

Title

Size
C

Document Number
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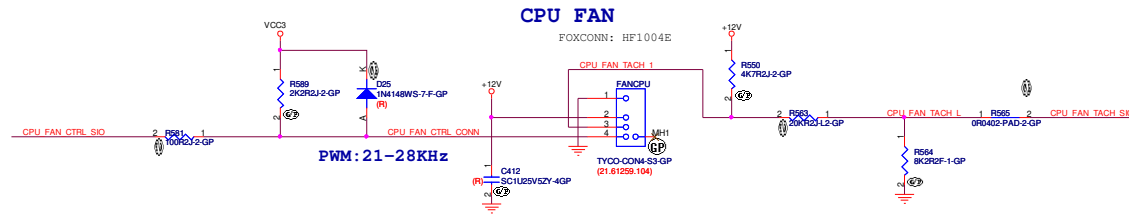
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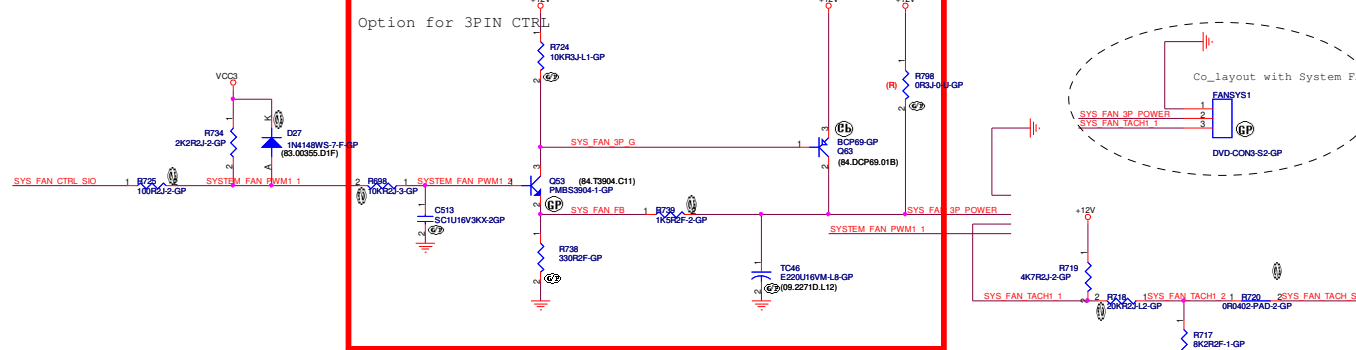
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SIO FAN CONTROL

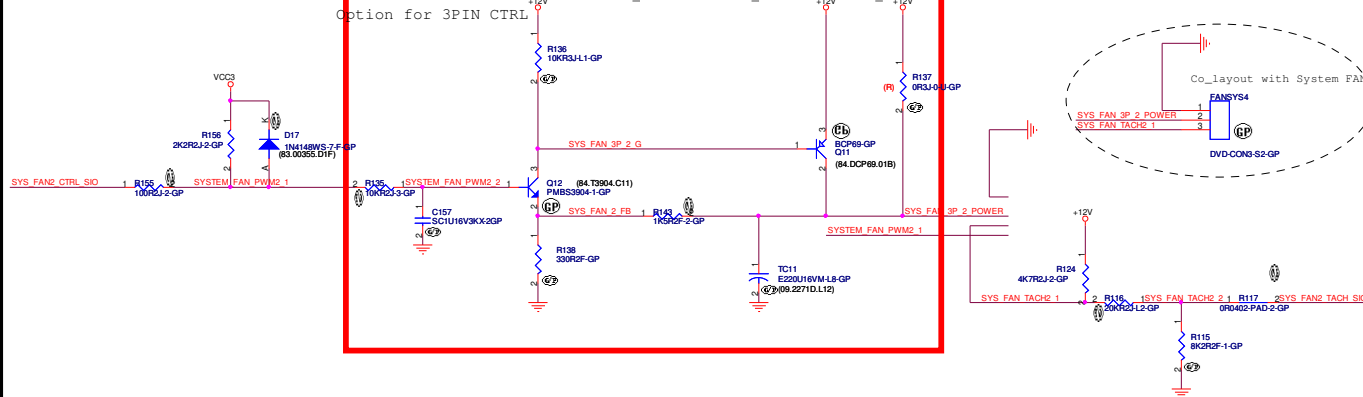
- 36 CPU_FAN_CTRL_SIO
- 36 CPU_FAN_TACH_SIO
- 36 SYS_FAN_CTRL_SIO
- 36 SYS_FAN_TACH_SIO
- 36 SYS_FAN2_CTRL_SIO
- 36 SYS_FAN2_TACH_SIO



SYS 3 PINS/4 PINS FAN CONTROL

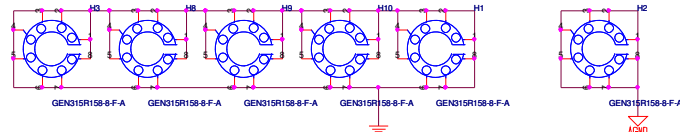
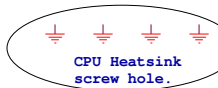


2nd SYS 3 PINS/4 PINS FAN CONTROL



PCB MOUNTING HOLES

Remove CPU Heatsink Screw Holes



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ONFI

PCIEX1

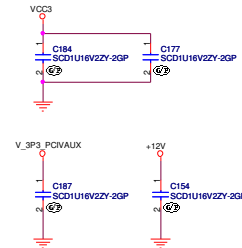
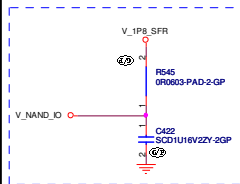
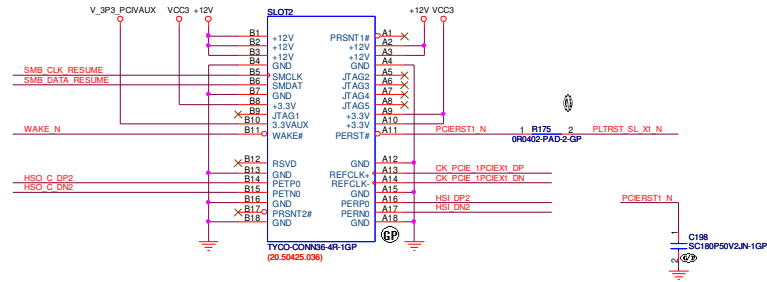
PCIEX1

PCIEX1

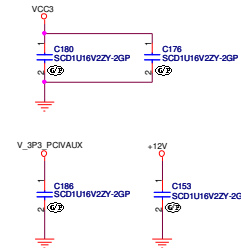
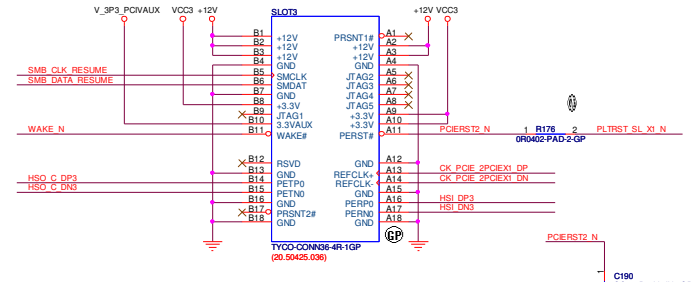
Others

35 PLTRST_SL_X1_N
19,26,32,36 SMB_CLK_RESUME
19,26,32,36 SMB_DATA_RESUME
19,26,32 WAKE_N

PCIEX1 CONN

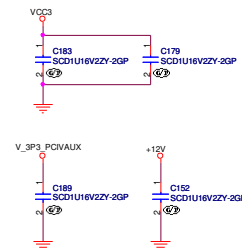
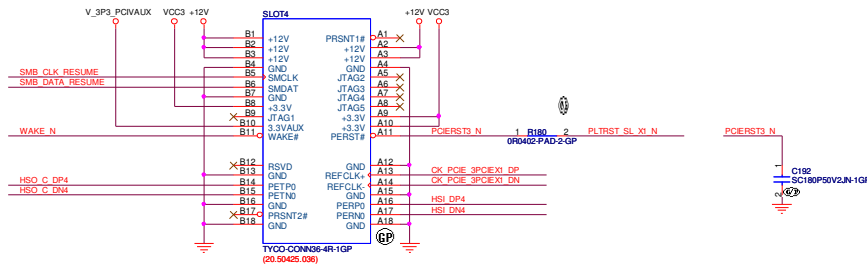


PCIEX1 CONN



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PCIEX1 CONN



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Date _____			
Time _____			
Rep. _____			


```

19 H_SLOT0CC_N      >>>
21 CHASSIS_ID_0     <<<
21 CHASSIS_ID_0     <<<
21 CHASSIS_ID_1     <<<
21 MTST_ID          <<<
21 FP_DETECT        <<<

36 PWR_LED_G        >>>
36 PWR_LED_Y        >>>

36 PWR_LED_CNTL     >>>
36 SUS_LED_CNTL     >>>

36 DIAG_LED1        >>>
36 DIAG_LED2        >>>
36 DIAG_LED3        >>>
36 DIAG_LED4        >>>

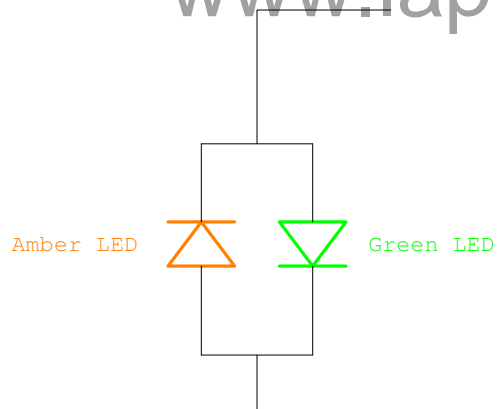
```

[illegible]

Schematic diagram of the SATA LED driver circuit. The circuit includes a MOSFET (2N7002-11-GP) with its gate connected to VCC3 through a 2N7002-E31 MOSFET. The MOSFET's drain is connected to a 10K R2J-3-GP resistor, which is then connected to VCC. The MOSFET's source is connected to ground. The MOSFET's drain is also connected to the SATA_LED_OUT signal. The MOSFET's gate is connected to PCH_SATA_LED_N.

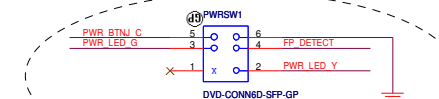
Prevent circuit

BIOS: Open-Drain
Default High, Output

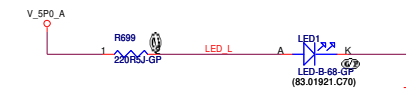


BIOS: Open-Drain
Default High, Output

```
2010/10/21
delete D29 diode
```



2010/10/28
Add PWRSW1 for Palm Beach



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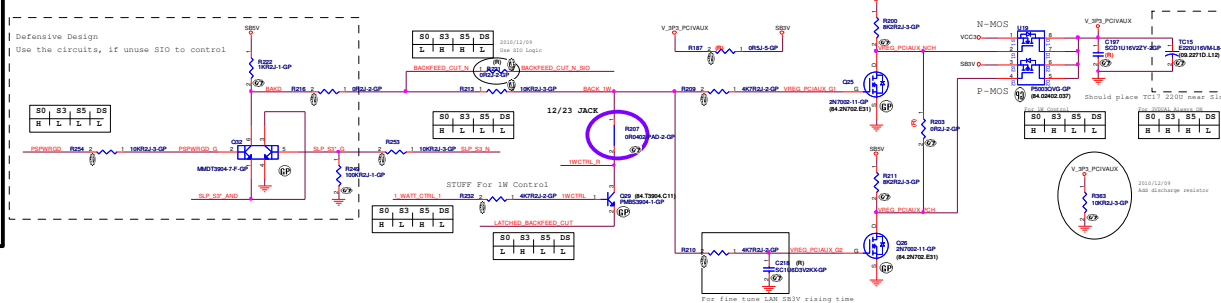
```

36.45 P5PWGRD >>>
19.36.45.46 SLP_53_N >>>
19 1_WATT_CTRL_1 >>>
19 SLP_LAN_N >>>

5 LATCHED_BF_CUT_SIO >>>
BACKFEED_CUT_N_SIO >>>

10.19 H_DRAMPWRD >>>
5 SUS_WARN_SVDUAL >>>
19 USB_PWR_CRL1 >>>
19.32 LAN_EN >>>
19.36.46 SLP_54_N >>>

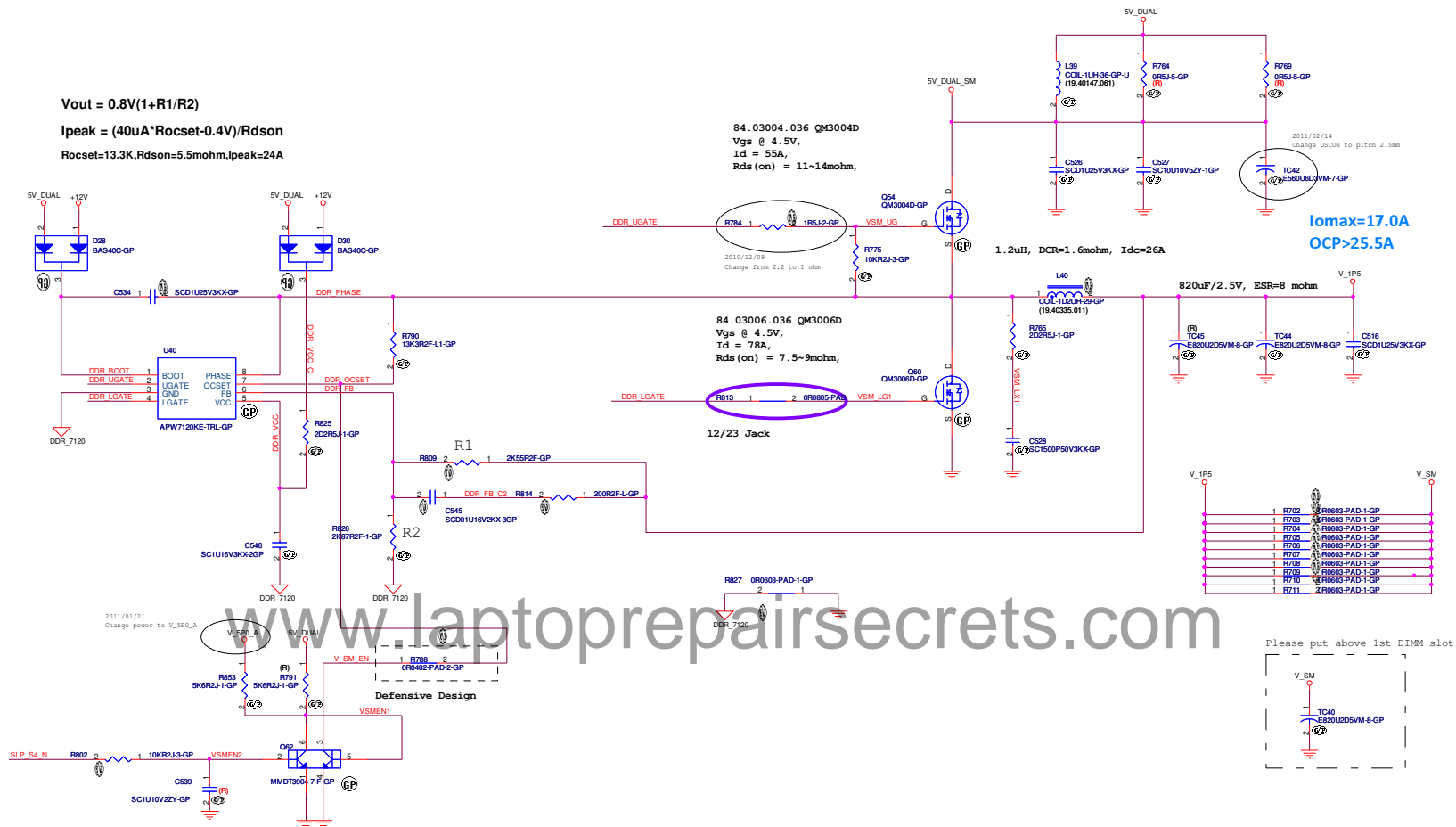
```

[illegible][illegible]

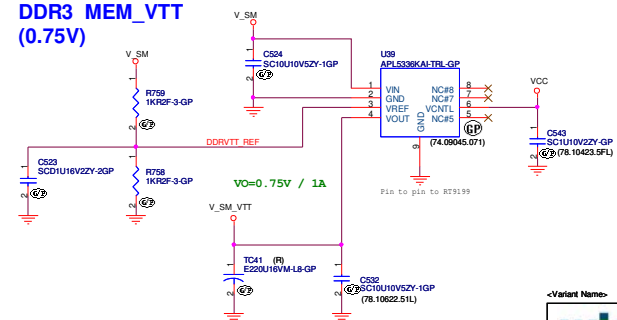
$$V_{out} = 0.8V(1+R1/R2)$$

$$I_{peak} = (40\mu A \cdot R_{ocset} - 0.4V) / R_{dson}$$

$$R_{ocset} = 13.3K, R_{dson} = 5.5m\Omega, I_{peak} = 24A$$



DDR3 MEM_VTT (0.75V)



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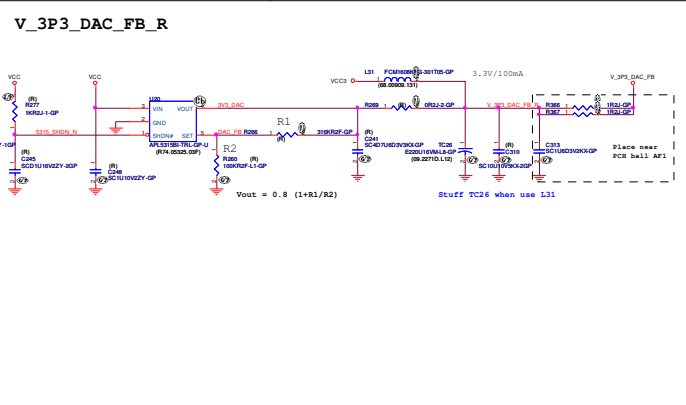
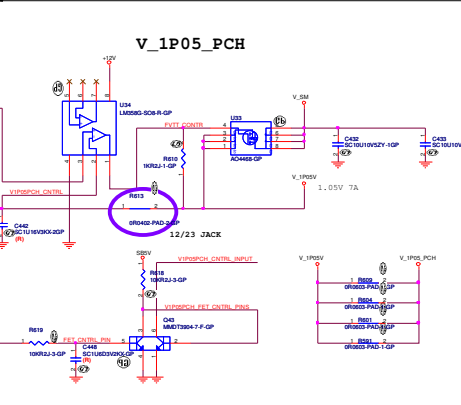
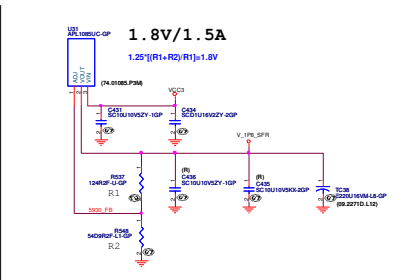
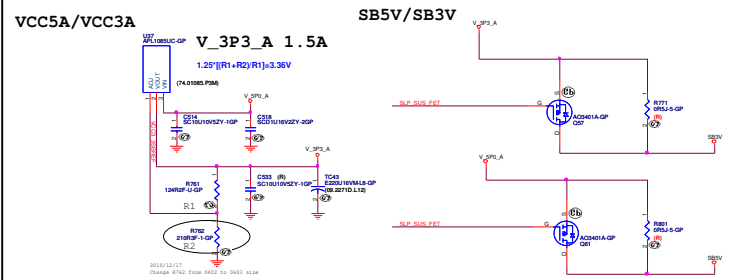
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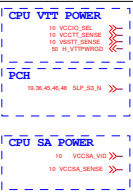
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Remove V_1P05_ME Circuit

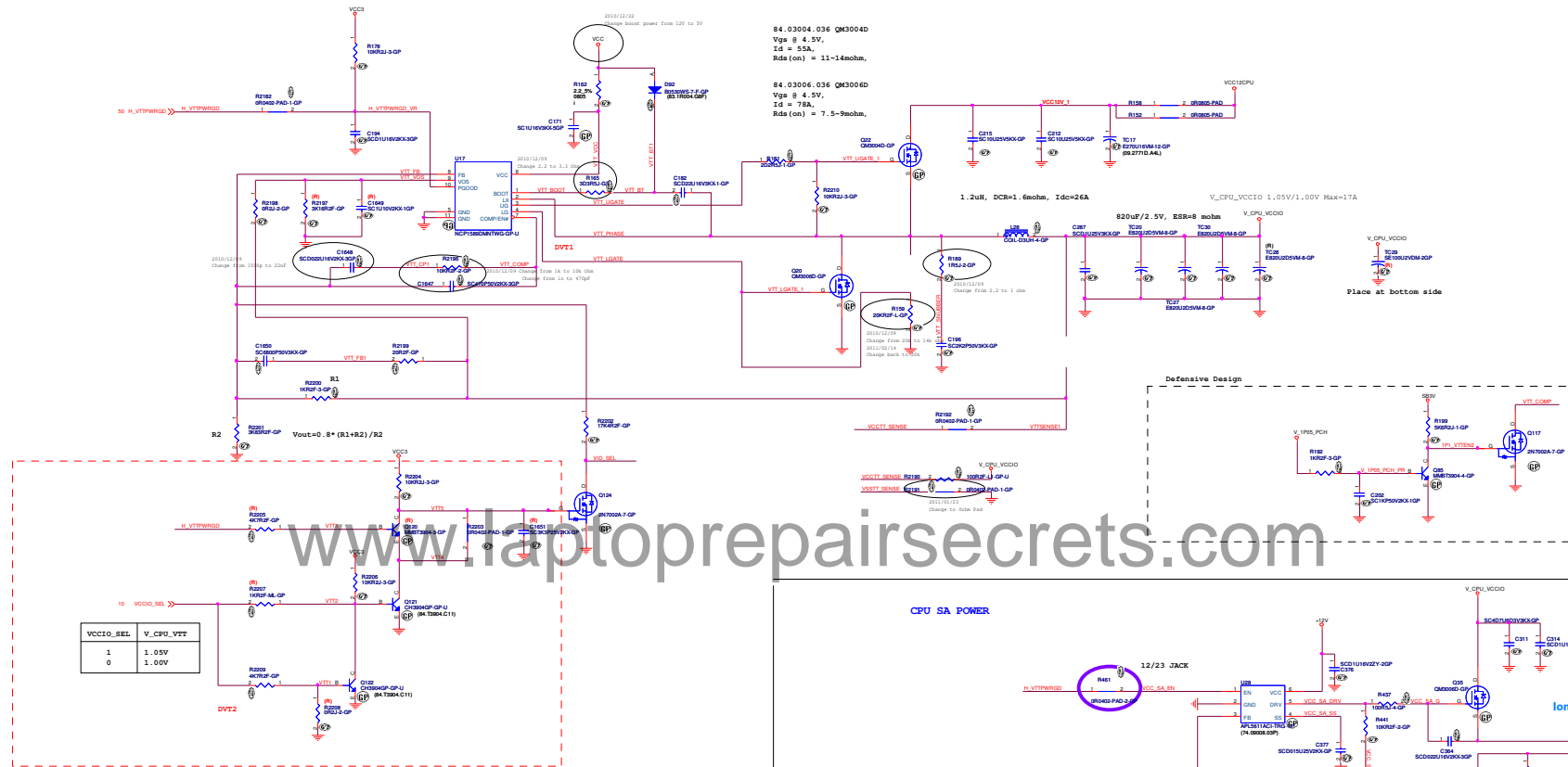
Remove ME Defensive Circuit



CPU VTT POWER

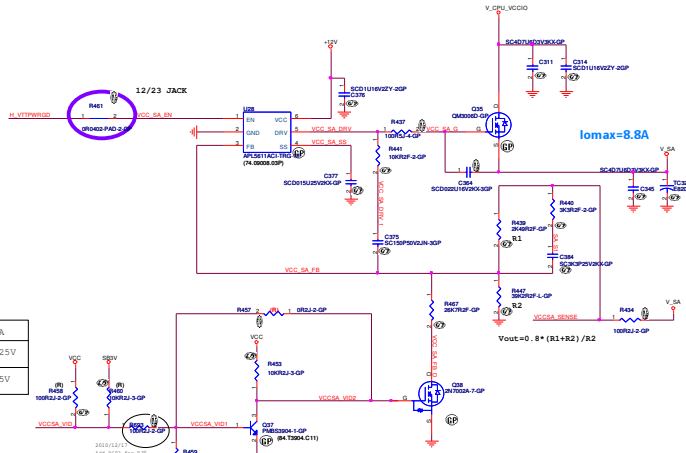
$I_{peak} = (8.5uA \cdot R_{ocset}) / (DCR \cdot K)$

$R_{ocset} = 6.49K, DCR = 1.6m\Omega, K = 1.3, I_{peak} = 26.5A$



CPU SA POWER

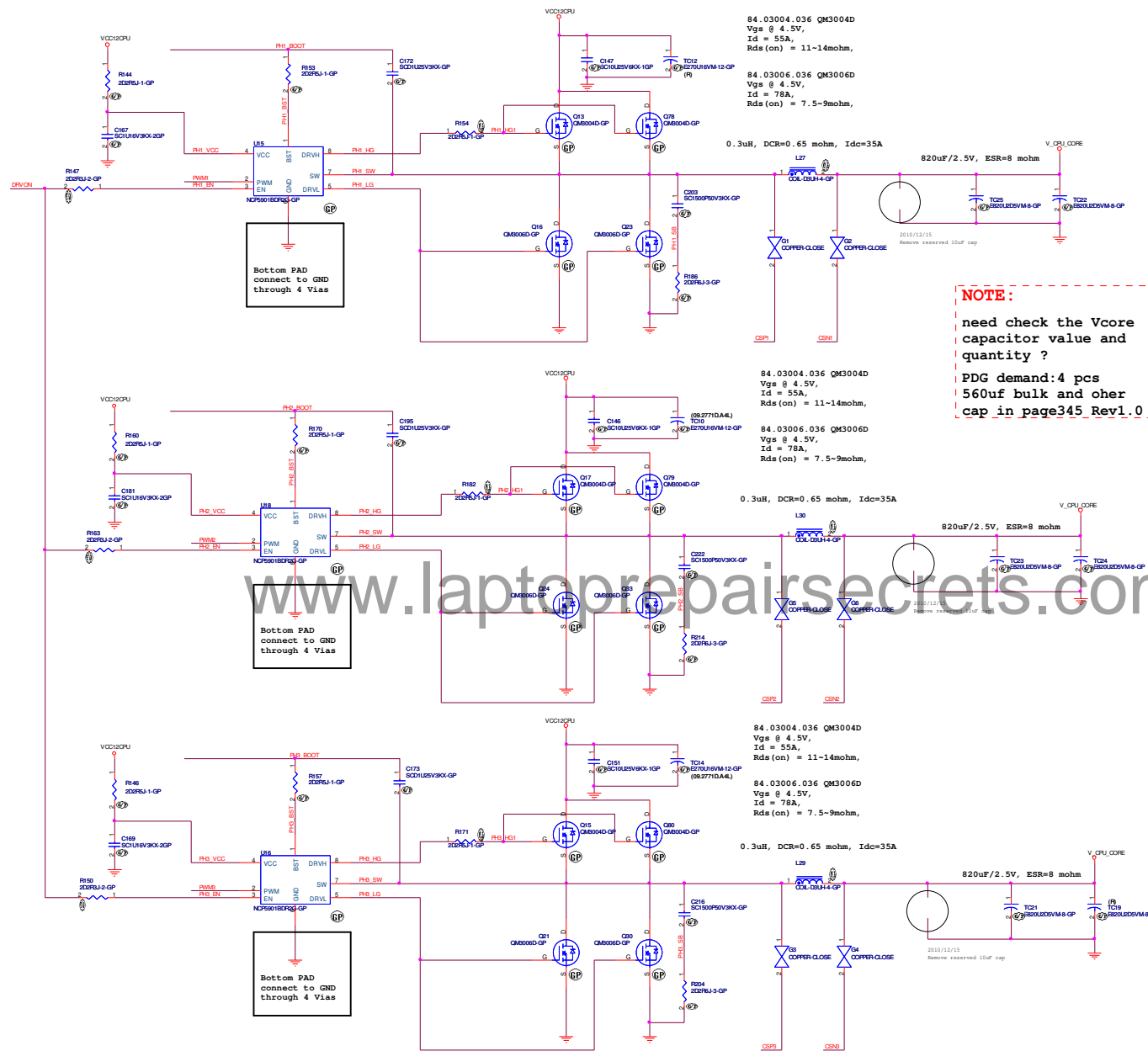
VCCSA_VDD	V_SA
0	0.925V
1	0.85V



CPU Vcore POWER

50 DRVON >>
50 CPM1 >>
50 CPM2 >>
50 CPM3 >>
50 CPM4 >>
50 CPM5 >>
50 CPM6 >>
50 CPM7 >>
50 CPM8 >>
50 CPM9 >>
50 CPM10 >>

VCC_CORE



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